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SPC-F005.DWG

REVISIONS

DOC. NO. SPC-F005 * Effective: 7/8/02 * DCP No: 1398

DCP #	REV	DESCRIPTION	DRAWN	DATE	CHECKD	DATE	APPRVD	DATE
1262	A	RELEASED	HO	9/5/02	JWM	9/5/02	DJC	9/6/06

Description: A PN Unijunction Transistor designed for use in pulse and timing circuits, sensing circuits, and thyristor trigger circuits.

Electrical Characteristics: ($T_A = +25^\circ\text{C}$ Unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF Characteristics						
Intrinsic Standoff Ratio		$V_{B2B1} = 10\text{V}$, Note 3	0.68	-	0.82	-
Interbase Resistance	r_{BB}	$V_{B2B1} = 3\text{V}$, $I_E = 0$	4.7	7.0	9.1	k Ohms
Interbase Resistance Temperature Coefficient			0.1	-	0.9	%/°C
Emitter Saturation Voltage	$V_{EB1(sat)}$	$V_{B2B1} = 10\text{V}$, $I_E = 50\text{mA}$, Note 4	-	3.5	-	V
Modulated Interbase Current	$I_{B2(mod)}$	$V_{B2B1} = 10\text{V}$, $I_E = 50\text{mA}$	-	15	-	mA
Emitter Reverse Current	I_{EB20}	$V_{B2E} = 30\text{V}$, $I_{B1} = 0$	-	0.005	0.2	μA
Peak Point Emitter Current	I_P	$V_{B2B1} = 25\text{V}$	-	1	2	μA
Valley Point Current	I_V	$V_{B2B1} = 20\text{V}$, $R_{B2} = 100\text{ Ohms}$	8	10	18	mA
Base-One Peak Pulse Voltage	V_{OB1}		6	7	-	V

Features:

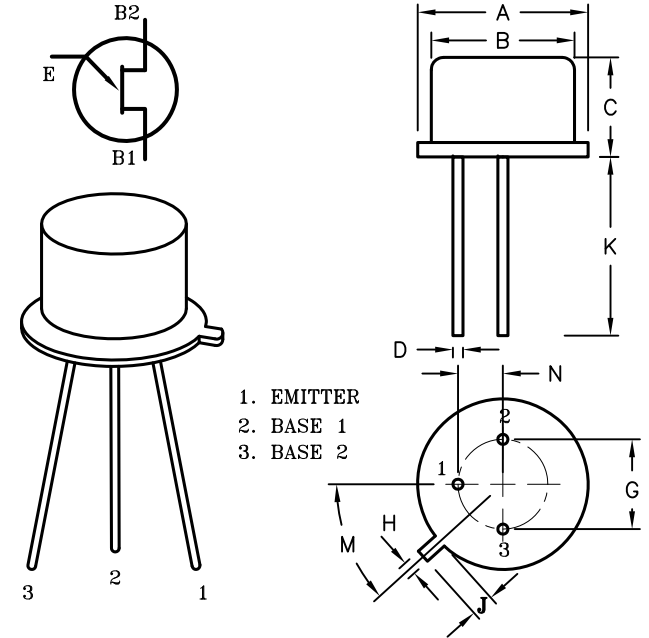
- low peak point current: $2\mu\text{A}$ (Max.)
- Low emitter reverse current: 200nA (Max.)
- Passivated surface for reliability and uniformity

ABSOLUTE MAXIMUM RATINGS: ($T_A = 25^\circ\text{C}$ Unless otherwise specified)

- Power Dissipation (Note 1) P_D : 300 mW
- RMS Emitter Current $I_{E(RMS)}$: 50mA
- Peak Pulse Emitter Current (Note 2), i_E : 2 Amps
- Emitter Reverse Voltage V_{B2E} : 30 Volts
- Interbase Voltage V_{B2B1} : 35 Volts
- Operating Junction Temperature Range T_J : $-65^\circ\text{C} \sim +125^\circ\text{C}$
- Storage Temperature Range T_{stg} : $-65^\circ\text{C} \sim +150^\circ\text{C}$

Notes:

- Derate $3\text{mW}/^\circ\text{C}$ increase in ambient temperature. The total power dissipation (available power to Emitter and Base-Tow) must be limited by the external circuitry.
- Capacitor discharge $-10\mu\text{F}$ or less, 30V or less.
- Intrinsic standoff ration is defined by the equation: $V_P = V_F / V_{B2B1}$
Where: V_P = peak Point Emitter Voltage; V_{B2B1} = Interbase Voltage; V_F = Emitter to Base-One Junction Diode Drop ($\sim 0.45\text{V}$ @ $10\mu\text{A}$)
- Use pulse techniques: Pulse Width $\sim 300\mu\text{s}$, Duty Cycle $\leq 2\%$ to avoid internal heating due to interbase modulation which may result in erroneous readings.



Dimensions	A	B	C	D	G	H	J	K	M	N
Min.	5.31	4.52	4.32	0.41	2.54	0.91	0.71	12.7	45°	1.27
Max.	5.84	4.95	5.33	0.48		1.17	1.22			

DISCLAIMER:
ALL STATEMENTS AND TECHNICAL INFORMATION CONTAINED HEREIN ARE BASED UPON INFORMATION AND/OR TESTS WE BELIEVE TO BE ACCURATE AND RELIABLE. SINCE CONDITIONS OF USE ARE BEYOND OUR CONTROL, THE USER SHALL DETERMINE THE SUITABILITY OF THE PRODUCT FOR THE INTENDED USE AND ASSUME ALL RISK AND LIABILITY WHATSOEVER IN CONNECTION THEREWITH.

TOLERANCES:
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE FOR REFERENCE PURPOSES ONLY.

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DRAWING TITLE: Transistor, Unijunction, TO-18, PN			
SIZE	DWG. NO.	ELECTRONIC FILE	REV
A	2N2647	35C0694.DWG	A
SCALE: NTS		U.O.M.: Millimeters	SHEET: 1 OF 1