Design Considerations for Implementing Circuit Protection Devices in PC Designs

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Despite the recent slowing of personal computer sales in North America and Europe, Worldwide sales have remained relatively consistent due to increased sales in Asia and India. According to a Dataquest projection of PC usage, the number of systems worldwide will exceed 150 million units in 2002 and shipment of desktop and mobile systems will grow at 16.1% compound annual growth rate (CAGR). The constant demand for personal computers requires that developers and OEMs continue to improve on designs in order to remain competitive.

One strategy that has proven to be effective in securing market share is reducing the size of the PC while improving the systems capabilities. As a result, the average system is capable of performing numerous tasks simultaneously without effecting the performance of the system. Designers have increased the number of external interfaces so users can have the luxury of utilizing more peripheral devices without having to disconnect one device to use another. "Plug & Play" interfaces such as USB, Fire Wire (IEEE 1394) and SCSI formats have become more and more common on PCs. One only has to look at the changes that have been implemented on systems over the past year to see that this is the case. The *Intel PC 1999* and *PC 2000 Design Guide* mandates that two USB ports be available on every PC's system board with most newer designs including up to eight.

So what does this mean for component manufacturers of circuit protection devices? Simply enough, more opportunities for circuit protection manufacturers who are seeing an increase in demand for their products. In addition to an increase in demand for devices to protect interface ports, component manufacturers are faced with the responsibility of developing smaller components to meet the space requirement of the newest computer designs.

For example, let us look at circuit protection of a standard USB port from a design engineer's point of view. Using the Microsoft *Windows Hardware Design Guide* as an example, it promotes that a USB lines provide suitable voltage and current protection without the need for replacement of suppression devices every time that an overcurrent or overvoltage condition occurs. Therefore, when selecting suppression devices, a component that is self-resetting is ideal in these conditions.

The Polymer Positive Temperature Coefficient device (PPTC) has gained much popularity as an overcurrent-limiting device in USB applications because of these properties. The PPTC device typically consists of a conducting polymer layer that separates two or more electrodes. PPTCs are rated similar to standard fuses that are rated in relation to a circuit's typical operating current. When this rated current is exceeded, the polymer layer will begin to heat. The polymer material will then begin to transition from a solid to a liquid state. As the polymer material expands, conductive layers within the polymer begin to break causing the device to shift from a low resistance state to a high resistance state (Figure 1). The resulting shift in the resistance of the device results in reducing nearly all of the current through the device. After a fault condition is removed, the polymer begins to contract and cool. During the cooling process the conducting chains come back into contact with each other restoring normal current flow through the device.

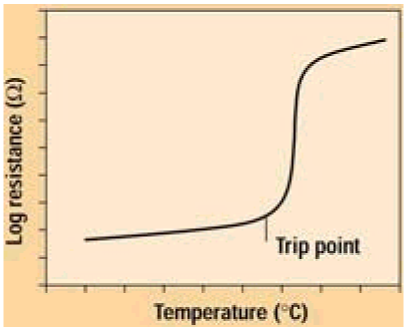


Figure 1. Graph of PTC performance with increasing heat caused by overcurrent.

It is obvious from a description of the PPTCs functional characteristics, why it has become the device of choice for overcurrent protection on USB ports. Now we should look a little further into the electrical response of a PPTC based on the electrical characteristics of a USB port.

USB Circuit Designs with PTC Overcurrent Protection
USB ports are configured as either self-powered or bus-powered. A self-powered USB hub must supply current up to 500 mA on all of its ports. The self-powered hub does not draw power from the USB stream but may utilize up to 100 mA from upstream devices or hubs to make functionality possible when it is powered down. Bus-powered hubs can draw up to 500 mA from an upstream self-powered connection. Typically, current of 100 mA is available for functions and processors internal to the hub. External ports in a bus-powered hub can supply up to 100 mA per port, with a maximum of four ports per hub.
Voltage-drop calculations for several applications of port protection in USB circuit designs are presented in Table I (Note: Device resistances reflect maximum on-board resistance of Littelfuse 1812L150PRT and 1812L260PRT PPTC devices). The calculations demonstrate the effect of several PPTC devices available to provide overcurrent protection. In the design of these ports, consideration must be given to ensuring that the voltage drop does not fall below the minimum of 4.75 V for a self-powered hub port, or 4.40 V for a bus-powered hub port. The upstream voltage supplied to a bus-powered hub is 4.75 V.

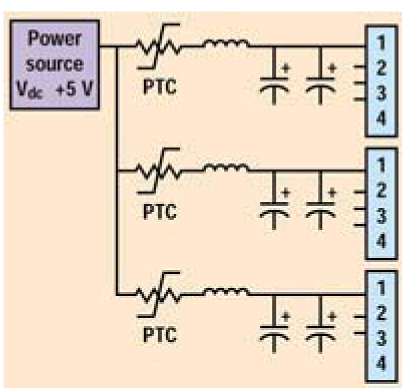


Figure 2: Self-powered Hub Individual Port Protection

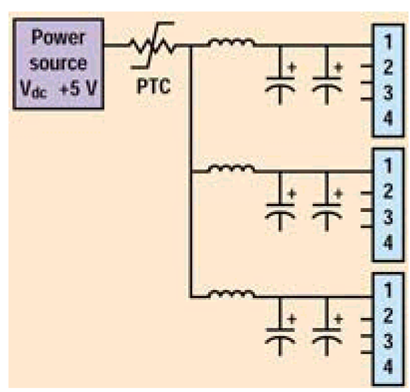


Figure 3: Self Powered Hub Multiple Port Protection

Self-powered hub (individual port, see Figure 2):			
Power supply			5.000 V
Trace	20 mΩ x 0.5 A	= 0.010 V	
Ferrite bead	5 mΩ x 0.5 A	= 0.003 V	

LF 1812L150 PTC	120 m Ωx 0.5 A	= 0.060 V	
V_{out}			4.933 V
Self-powered hub (multiple port [2], see Figure 3):			
Power supply			5.000 V
Trace	(10 mΩ x 1.0 A) + (10 mΩ x 0.5 A)	= 0.015 V	
Ferrite bead	5 mΩ x 0.5 A	= 0.003 V	
LF 1812L150 PTC	120 mΩ x 1.0 A	= 0.120 V	
V_{out}			4.862 V
or			
Self-powered hub (multiple port [2], see Figure 3):			
Power supply			5.000 V
Trace	(10 mΩ x 1.0 A) + (10 mΩ x 0.5 A)	= 0.015 V	
Ferrite bead	5 mΩ x 0.5 A	= 0.003 V	
LF 1812L260 PTC	50 mΩ x 1.0 A	= 0.050 V	
V_{out}			4.932 V
Self-powered hub (multiple port [3], see Figure 3):			
Power supply		5.000 V	
Trace	(10 mΩ x 1.5 A) + (10 mΩ x 0.5 A)	= 0.025 V	
Ferrite bead	5 mΩ x 0.5 A	= 0.003 V	
LF 1812L260 PTC	50 mΩ x 1.5 A	= 0.075 V	
V_{out}			4.897 V
Bus-powered hub (individual port, see Figure 4):			
Supply voltage			4.750 V
Cable	190 m Ωx 0.5 A	= 0.080 V	
Trace	(10 mΩ x 0.4 A) + (10 mΩ x 0.1 A)	= 0.005 V	
Ferrite bead	5 mΩ x 0.1 A	= 0.001 V	
MOSFET	80 mΩ x 0.4 A	= 0.032 V	
LF 1812L150 PTC	120 mΩ x 0.1 A	= 0.012 V	
V_{out}			4.620 V
Bus-powered hub (multiple port [2], see Figure 5):			
Supply voltage			4.750 V
Cable	190 mΩ x 0.5 A	= 0.080 V	
Trace	(10 mΩ x 0.4 A) + (10 mΩ x 0.1 A)	= 0.005 V	
Ferrite bead	5 mΩ x 0.1 A	= 0.001 V	
MOSFET	80 mΩ x 0.4 A	= 0.032 V	
LF 1812L260 PTC	120 mΩ x 0.2 A	= 0.010 V	
V_{out}			4.622 V
Bus-powered hub (multiple port [4], see Figure 5):			
Supply voltage			4.750 V
Cable	190 mΩ x 0.5 A	= 0.080 V	
Trace	(10 mΩ x 0.4 A) + (10 mΩ x 0.1 A)	= 0.005 V	
Ferrite bead	5 mΩ x 0.1 A	= 0.001 V	
MOSFET	80 mΩ x 0.4 A	= 0.032 V	
LF 1812L260 PTC	50 mΩ x 0.4 A	= 0.020 V	
V_{out}			4.612 V

Table I. Sample calculations of voltage drop for various applications of port protection in USB

Circuit Designs.

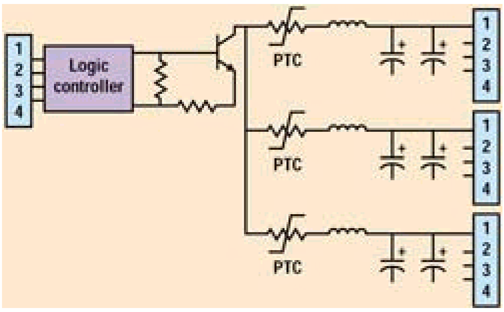


Figure 4: Bus Powered Hub Individual Port Protection

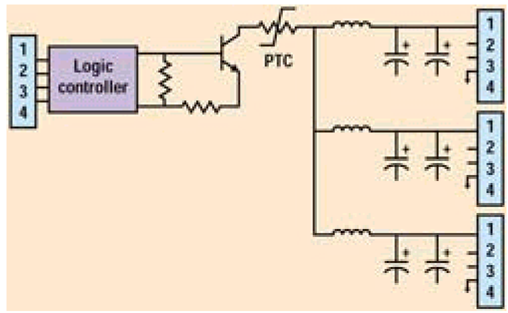


Figure5: Bus Powered Hub Multiple Port Protection

Bus-powered-hub calculations include a resistance budget for the connecting cable. The USB standard specifies that connection cables from host to hub and peripherals have a maximum length of 5 m and a maximum resistance of 190 mΩ. The circuit trace was assumed to be 4 in., with a trace resistance of 5 mΩ /in. A 5-mΩ ferrite bead and two capacitors used for EMI suppression are illustrated in the circuit diagrams. Bus-powered circuits include control logic circuitry (a field-effect transistor with 80-m resistance) which enables software control of bus power and port reset capabilities.

Overcurrent circuit protection scenarios in Figures 2 through 5 depict individual-port and multiple-port (ganged) protection for self-powered hubs and bus-powered hubs. Individual-port protection offers an advantage over ganged port protection in that if one port fails, the other ports are unaffected. Additionally, the time-to-trip parameter that PPTCs inherently demonstrate allows the design engineer to eliminate false circuit trips due to power-on currents. The calculations show that the voltage drop for overcurrent protection with PTC devices complies with the requirements in the USB specifications.

Overvoltage Protection of USB1.1 Port

There are significant transmission rate differences between the future version 2.0 and the current version 1.1 of the USB specification. The data rates are 480mbps and 12 mbps respectively. This allows other Littelfuse technologies with higher capacitance to provide the recommended protection solution. Figure 6 is utilizing the Littelfuse Multilayer Varistor technology providing an economical solution of not only data line protection but also the power rail. In addition, Figure 7 shows a Littelfuse silicon solution providing fully integrated protection of the data line and power rail in a 4 lead SOT-143 package. Using Silicon is an economical solution to provide the lowest clamp voltage to protect the more sensitive signal lines.

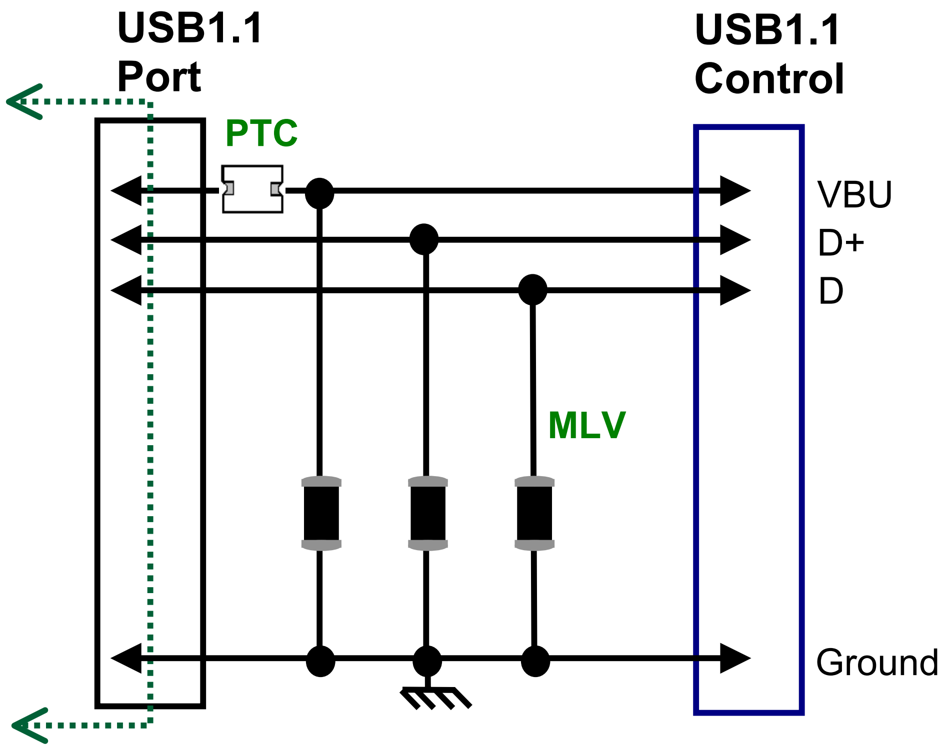


Figure 6: USB 1.1 Protection Using Multilayer Varistors

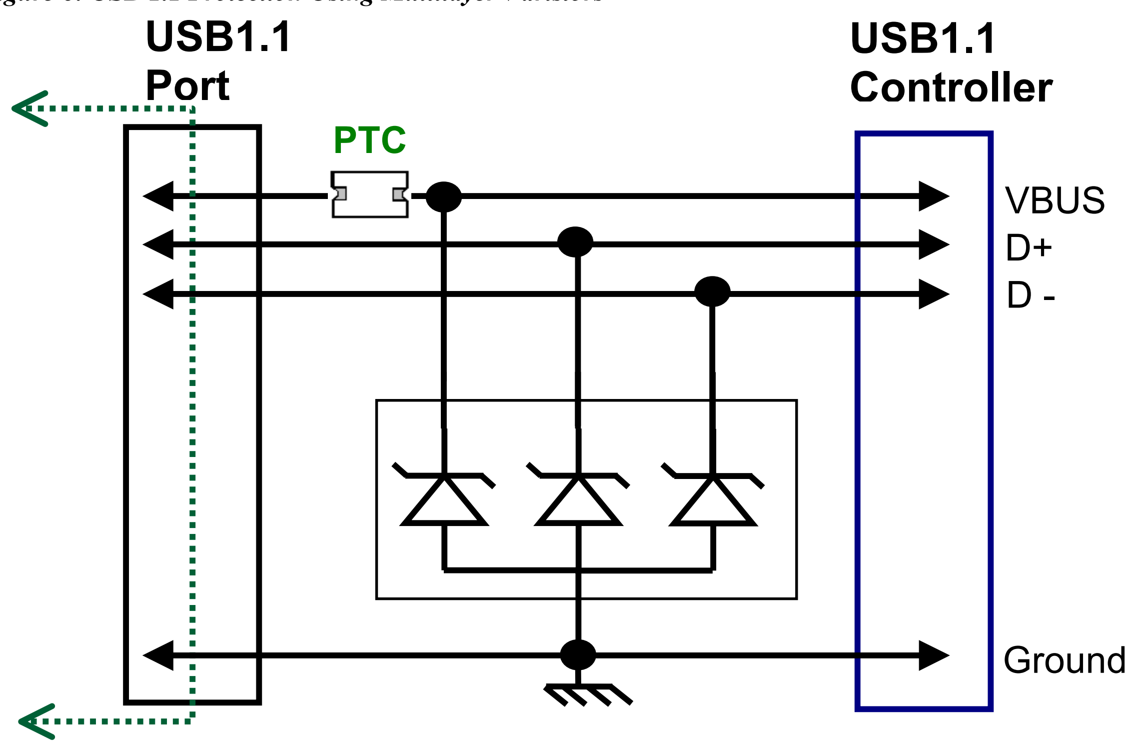


Figure 7: USB 1.1 Protection Using Diodes

Overvoltage Protection of USB 2.0 Port
Data transmission lines of USB 2.0 ports are also susceptible to damage that result from Electrostatic Discharge (ESD) events. ESD events are very fast events that reach peak voltages (up to 25 KV) in less than 1 nanosecond. Many circuit designers have developed overvoltage protection on interface ports due to the frequency of these events. As a result of technology developed through the development of PPTC devices, new and effective methods of diverting voltage spikes can be inexpensively implemented into circuit designs. In this example we will look at the Littelfuse PulseGuard® suppressor line of ESD protection. In the case of USB line protection, the PGB002ST23 is ideal as it can protect both data lines in a .120” x .090” package. These devices are connected between the data lines and ground producing a high resistance state between the data lines and ground (Figure 8). This high resistance state is necessary, especially in USB 2.0 controllers, so that the device is transparent to the data being transmitted.

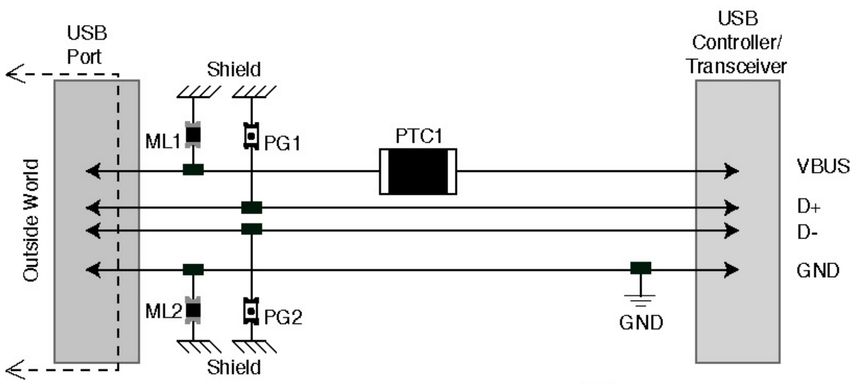
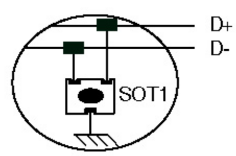


Table 1. Symbol Definition

	Shield (Chassis Ground)
	GND (Signal Ground)
PTC 1	1206L/1812L Series Resettable PTC
ML1, 2	V5.5MLA0603
PG1, 2	PGB0010603
SOT1	PGB002ST23
	Physical Tie



Option:
SOT23 PulseGuard Surface Mount
ESD Suppressors provide High
Speed Data Line Protection on both
D+ and D- lines in one package

Figure 8: Device Layout on USB 2.0 Circuit using both overcurrent and overvoltage protection.

Another important consideration when selecting a voltage protection device is the fact that as the speed of a transmission signal increases, the effects of the device capacitance become more obvious. The greater the capacitance of a device, the more likely that signals will become distorted at high speeds. Therefore a device should have as little capacitance as possible. The device referenced above has a capacitance of less than 1 pF, making it transparent in the electric circuit of a USB 2.0 port.

When an ESD transient develops, the suppressor resistance drops sharply. Therefore, the resulting low resistance shunts the ESD current spike away from the circuit (Figure 9). After the energy is dissipated, the suppressor automatically returns to its normal high resistance state, once again becoming transparent to the circuit.

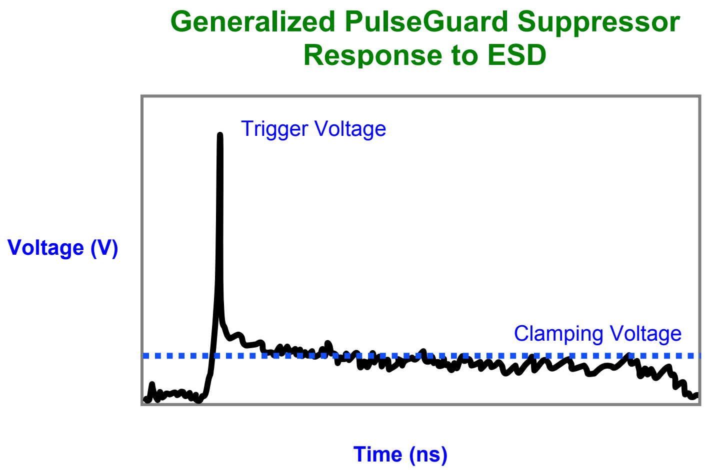


Figure 9. ESD Waveform

Size Constraints and Circuit Protection Devices
As touched on earlier, PC designers are continually finding themselves in the position of reducing system designs while increasing capabilities. As a result circuit board real estate becomes more and more valuable. Suppression device manufacturers are faced with the task of providing the same reliability in their devices while reducing the package sizes to minimize the space required to implement these devices into designs. Several years ago surface mount PPTCs were implemented into a 3425 (.340" x .250") package. The surface mount designs improved speed of soldering while reducing space requirements. Today, the 1812 (.180" x .120") package is the most commonly used for port protection. Currently, Littelfuse, Inc. now offers a 1206 (.120" x .160") line of surface mount fuses as the onboard space that is required is 1/3 of that used by an 1812 series of device. In addition to computer application, the reduced size allows for implementation in circuit designs that were too space-constrained for PPTC devices.

Similarly, the ESD devices referenced earlier are following the same trend. The PulseGuard multi-line device that comes in a SOT23 package size is also available for single-line applications in a 0603 (.060" x .030") package. Currently, 0402 devices are being developed to further reduce the consideration that designers must make when using these devices in their designs. However, as "Plug and Play" application continue to become more and more common in desktop and portable PCs, the demand for these products will continue to grow. More importantly the technological advancements of component and system manufacturers will continue to push the other to develop smaller and more complex designs.

References:

- Computer Markets for Passive Components

Paumanok Publications, Inc. 1998
Electronic Circuit Protection Components: World Markets

- Technologies & Opportunities: A 2000-2005 Analysis

Paumanok Publications, Inc. 2000
PTC Overcurrent Protection for Universal Serial Bus Circuit Designs

- Rick Hapanowicz

Compliance Engineering Magazine
May/June 2000

- John Norris

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