

Novel Power MOSFET Packaging Technology Doubles Power Density in Synchronous Buck Converters for Next Generation Microprocessors

Andrew Sawle, Carl Blake and Dragan Mariæ
International Rectifier

as presented at APEC 2002

Abstract: *This paper will introduce a novel power packaging technology developed by International Rectifier. This new packaging technology breaks ground in reducing package related losses and thus allowing designers to develop power supplies capable of meeting the demands of latest generation processors.*

I. INTRODUCTION

Ever increasing demands for processing power has seen companies such as Intel and AMD relentlessly self-obsolting themselves with faster and more powerful processor chips. These advances have, in general, been made through increases in the density of transistors that can be made on a given area of silicon. Consequently each successive processor generation employs millions more transistors than the previous. Whilst this boosts the number of operations that can be carried out every second, it also means that the current required by the processor to do this must increase. Current requirements for processors have increased exponentially over the last 4-5 years and will soon be exceeding 100Amps in a number of processor applications.

The challenge has been laid firmly at the door of the designers of the power supplies that service the processors. The common approach being taken is to employ multiphase converters to achieve the escalating current levels. For example, a four-phase converter running 25A per phase will supply 100A total. By running a phased converter and also increasing the operating frequency to satisfy the fast transient response required by processors running at higher clock speeds it is possible to reduce the size of the passive components used. This helps to ensure that the converter does not have to increase in size proportionally to the increase in current. However, this does mean that power densities on boards are increasing and the issue of cooling the power components within the converter is becoming a major issue.

Reducing the losses exhibited and consequently power dissipated in the power components, e.g., the MOSFETs, has therefore been the focus of power supply

designers and component vendors alike. The evolution of power MOSFET silicon has radically cut both on-state and switching losses. However, power packaging is now becoming the limiting factor with the losses attributed to the packaging in some cases being greater than the losses from the silicon itself. Over the last couple of years there has been a move to reduce these package related losses. This paper introduces a new packaging technology, DirectFET™, targeted for processor power converters. This new technology radically cuts conduction losses, whilst facilitating improved cooling regimes to enable the current and power levels required by the next generation of processors. The paper will describe this new technology and illustrate the advances made with examples from in circuit evaluations before addressing the expected reliability of this platform. This new package is shown in Figure 1.0 below.



FIGURE 1.0 DIRECTFET™ TECHNOLOGY

II. DIRECTFET™ TECHNOLOGY

DirectFET™ technology has been designed and developed with the following objectives in mind:

1. Reduce the electrical resistance of the package to a level insignificant relative to the MOSFET $R_{ds(on)}$
2. Reduce the thermal impedance of the package, both junction to board and junction to topside of the package for dual side cooling applications.

3. Facilitate simplified board layout and paralleling of devices.
4. Enable the use of existing surface mount assembly lines and technology.

In order to achieve points 1 and 2 above, the design of DirectFET™ technology has rationalised some of the concepts and materials that are commonly used in power packaging. This simplified approach is shown as a cross section in Figure 2.0.

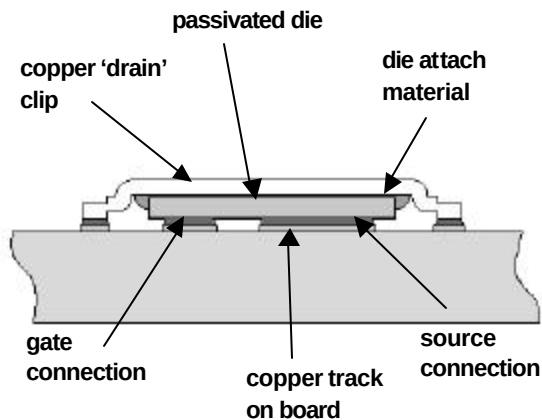


FIGURE 2.0 – CROSS SECTION OF DIRECTFET™ TECHNOLOGY

The cross section in Figure 2.0 shows a MOSFET die with the source face of the die soldered directly to the printed circuit board. The drain connection is then made from the back of the die to the board through the use of a copper 'can' into which the die has been bonded. The facilitator in this scheme is a new proprietary passivation system developed by International Rectifier. This passivation is applied to a wafer that has a solderable top metal stack (rather than an aluminium top metal commonly used for wirebonded devices). It is then patterned to open out solderable areas on the surface of the die for the source and the gate connections. This allows the shape of the solder joints between the silicon and the circuit board to be closely controlled. The passivation has two very important roles to play:

1. The passivation itself is unsolderable. This means that whilst allowing close control of the shape of the solder joints it also prohibits solder shorting between the gate and source contacts during the board mount process.
2. The passivation provides environmental protection for the termination structure and gate busses on the die. It is resistant to moisture and ionic contamination that may be found on the board or in the solder flux, etc.

With this passivation applied, the gate and source connections can be made directly between the circuit board and the die without any unnecessary leadframe or wirebonds in series with the conduction path. Since the

construction of the MOSFET silicon used in DirectFET devices is not that of a flipchip, *i.e. not all the connections are on a single side of the die*, the drain does require a 'leadframe connection' to complete the electrical circuit. The die is bonded into a copper clip or 'can' using a silver filled epoxy and the finished, fully tested device can be board mounted in the same way as any conventional surface mount component.

III. CONDUCTION PERFORMANCE

The rationalised approach taken with DirectFET™ technology has greatly reduced the conduction path through the package and removed the high resistance elements. Figure 3.0 shows a comparison of the conduction paths of this new technology versus older SO-8 and newer Copperstrap™ SO-8 packages. The comparison shows that DirectFET technology has eliminated conduction paths and material interfaces which all add resistance in series with the silicon die. The effect is that the die free package resistance has been reduced to less than $200\mu\Omega$, a reduction of 86% over the SO-8 & approximately 74% over the Copperstrap™ SO-8. This reduction in the series resistance means that in an SO-8 outline typical $R_{ds(on)}$ values of $2m\Omega$ are achievable.

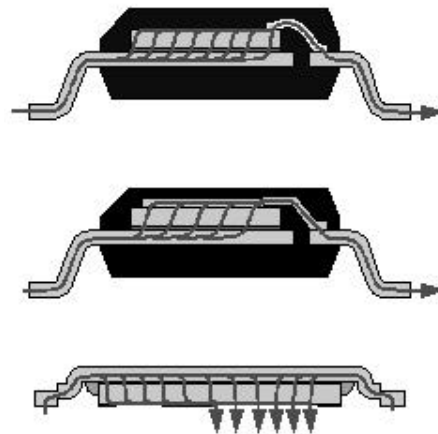


FIGURE 3.0 CONDUCTION PATHS FOR SO-8 (TOP), COPPERSTRAP™ SO-8 (MIDDLE) AND DIRECTFET™ TECHNOLOGY (BOTTOM)

IV. THERMAL PERFORMANCE

Whilst advances in conduction performance are key to increasing the current density in power converters, the issue of how to most effectively extract the heat from these converters and thus increase power density still applies. The direct nature of the coupling of the silicon to the board means that DirectFET technology has reduced the thermal resistance to the board. The thermal resistance from junction to board of a standard SO-8 package is of the order of 20°C/W . However DirectFET™ technology reduces this to 1°C/W as the thermal resistance path runs through the top metal and

the board attach solder only. This more effective cooling to the board increases the amount of power that can be dissipated for a given junction temperature. However, as power densities increase there comes a point beyond which it is not possible to dissipate any more power into the board as it effectively becomes saturated. In order for power densities to increase further it is necessary to take the heat away from the power device but not through conduction into the board. Most surface mount components cater only for heat transfer into the board with minimal additional heat transfer to the ambient through radiation and convection. The construction of DirectFET technology has radically reduced the heat conduction path to the top side of the package. The thermal resistance from the junction of the MOSFET to the top of the package is $3^{\circ}\text{C}/\text{W}$ compared to $25^{\circ}\text{C}/\text{W}$ for an SO-8. Predominantly this reduction is borne from the lack of moulding compound. This now means that dual sided cooling can realistically be employed in order to pull even more heat out of the device and increase the amount of power that can be safely dissipated. Dual sided cooling can take a number of different forms, three of these are shown in Figure 4.0.

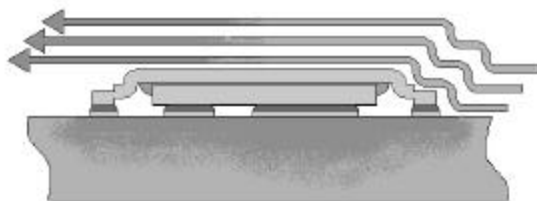


FIGURE 4.0A – EXAMPLES OF DUAL SIDED COOLING
FORCED AIR – NO HEATSINK

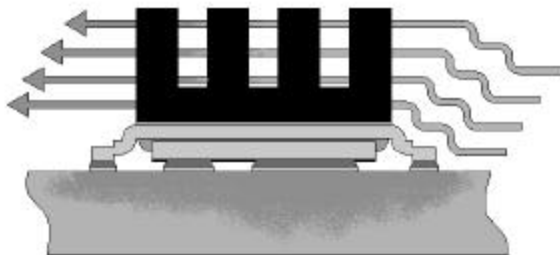


FIGURE 4.0B – EXAMPLES OF DUAL SIDED COOLING
FORCED AIR WITH ADDED HEATSINK

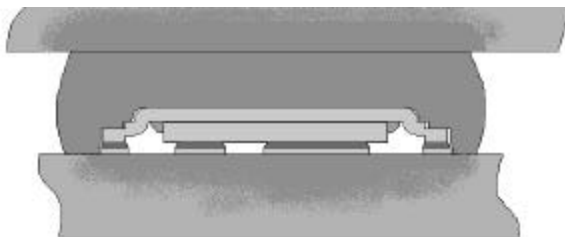


FIGURE 4.0C – EXAMPLES OF DUAL SIDED COOLING
SINKING TO CHASSIS THROUGH GAP-FILLING PAD

By using dual sided cooling it is possible to reduce the total thermal resistance from junction to ambient to less than $12^{\circ}\text{C}/\text{W}$. This figure, when

combined with the low conduction losses, means that it is possible to conduct greater than 30A with a single SO-8-outlined DirectFET technology device. The following section describes the results of in circuit evaluations that show the performance gains from the combined thermal and electrical improvements.

V. IN CIRCUIT EVALUATION RESULTS

In circuit performance evaluations have been carried out comparing the thermal and conduction performance of DirectFET technology to an SO-8 device utilizing the same silicon technology.

The thermal images in Figure 6.0 show a comparison of a 30Vn SO-8 (IRF7822) and a DirectFET technology device (IRF6603) both in the synchronous FET socket in a synchronous buck converter, running at $f_{\text{sw}}=300\text{kHz}$. In both cases the FETs are conducting 18A.

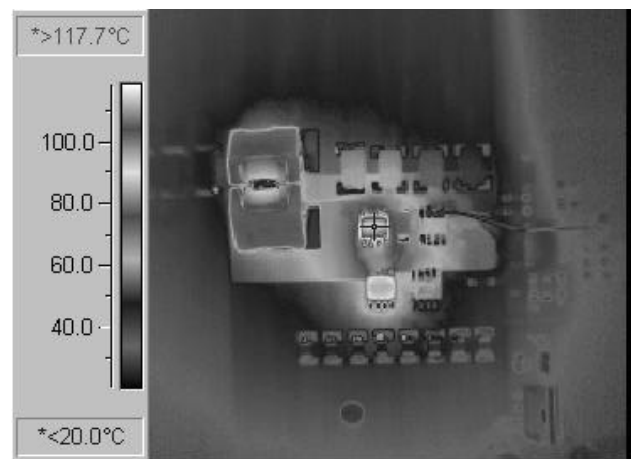


FIGURE 6.0A – THERMAL IMAGES OF SO-8 RUNNING AT 300KHZ, 18A –
TJ MEASURED AT 125°C IN SYNC-BUCK CIRCUIT

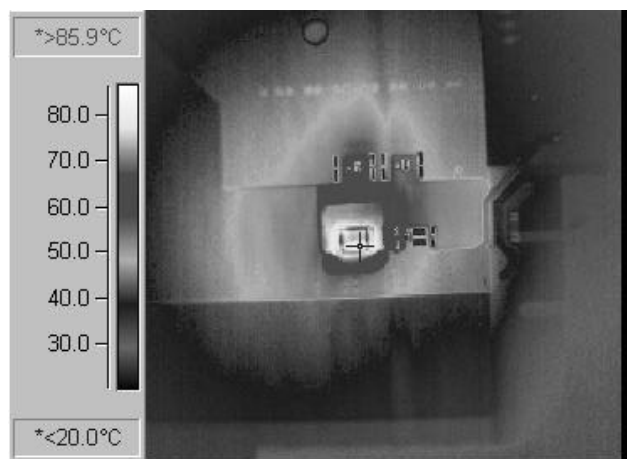


FIGURE 6.0B – THERMAL IMAGES OF DIRECTFET TECHNOLOGY
RUNNING AT 300KHZ, 18A – TJ MEASURED AT 75°C IN SYNC-BUCK
CIRCUIT

The comparison shown in Figure 6.0 is with no dual sided cooling, heat only being transferred into the board. The SO-8 image shows the heat contours concentrated closely around the device, which means that minimal heat is being dissipated into the board leading to a high junction temperature. Conversely the DirectFET technology image shows the contours spreading more widely around the device showing more heat being transferred into the board. Consequently for the same current the DirectFET device is running 50°C cooler than the SO-8. In application this would either mean that the DirectFET device could be run cooler than the SO-8 and hence greater reliability could be expected or more likely a greater current would be conducted for the same junction temperature. A set of evaluations were conducted to determine the maximum current which could be conducted for a peak board temperature of 105°C, a temperature commonly used as a limit in converter applications on FR4 substrate. The evaluations investigated cooling to board, 200 linear feet per minute airflow (no additional sink) and cooling to a chassis substitute. The results are shown in Table I.

	SO-8, IRF7822 in SyncFET socket	DirectFET, IRF6603 in SyncFET socket	%age increase in current
No topside cooling	18A	24A	33%
Constant 200LFM	20A	26A	30%
Heatsink to chassis substitute	22A	32A	45%

TABLE I – MAXIMUM MEASURED CURRENT FOR DIFFERING COOLING SOLUTIONS

In every case the DirectFET technology conducted at least 30% more current than the equivalent footprint SO-8 for the same cooling conditions. In fact, the DirectFET device case with the minimal cooling conditions conducted more current than the SO-8 with the best sinking solution.

VI. EFFICIENCY MEASUREMENTS

Improvements in both the thermal and conduction performance bring with them gains in converter efficiency. Measurements of efficiency were made for each of the cooling solutions shown in Table 1.0 for varying load current. The efficiency curves for DirectFET technology parts in both the synchronous FET socket and the control FET socket, both cooled and uncooled versus uncooled SO-8 devices are shown in Figure 7.0.

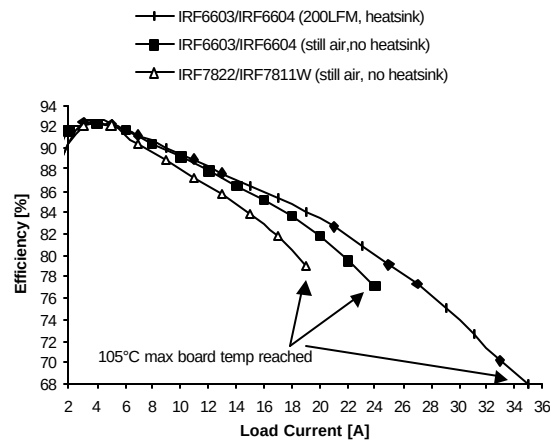


FIGURE 7.0 – EFFICIENCY CHART COMPARING DIRECTFET (IRF6603/4) WITH SO-8 (IRF7822/11) IN SYNCHRONOUS RECTIFIER CIRCUIT AT 300KHZ

The measurements in Figure 7.0 show the converter efficiency versus load current. In all cases the measurements were stopped at a current level where the maximum board temperature of 105°C was reached. It can be seen that at 18A the uncooled DirectFET devices give a four percentage point improvement in converter efficiency over the uncooled SO-8s. By heatsinking the DirectFET devices to a chassis substitute a further one percentage point improvement in converter efficiency was achieved at 18A. Alternatively the load current could be increased by 5.5A for the same converter efficiency, an increase of 30%. An additional point to note is that the improved cooling means that the converter could be run to 35A before the board temperature reached the 105°C limit. It is also important to note that the circuit used here was optimised for SO-8 devices. Namely, optimising the circuit for the DirectFET™ devices (e.g., using a high current inductor) would render noticeably higher efficiency at high current levels.

VI. CURRENT DENSITY INCREASES

The in circuit evaluations have shown that 30A is achievable using a single DirectFET technology pair (synchronous and control FET) whilst maintaining a maximum board temperature of 105°C. In order to achieve 30A it would be necessary to parallel two or more SO-8 devices in each of the synchronous and control FET sockets. Table II below shows a DirectFET technology versus SO-8 comparison of required board area and the resulting amps/in² for 30A per phase converters. To make a fair comparison it is assumed that both the DirectFET devices and the SO-8s are heatsinked to a chassis. In practice it would not be sensible to sink the SO-8 to a chassis in this application as the

performance gain through doing so would still not mean that a single device could be used.

Power Supply Solution	Area [in ²]	Amps/in ²
SO-8 2-phase solution	5.54	10.82
SO-8 4-phase solution	10.45	11.48
DirectFET 2 -phase solution	2.77	21.67
DirectFET 4 -phase solution	4.90	24.49

TABLE II. CURRENT DENSITIES FOR A 30A/PHASE SYNCHRONOUS BUCK CONVERTER

Table II shows that in both the two phase and the four phase solutions the current density has been doubled through the use of DirectFET technology. Also, as power is a function of current, the power density is also doubled in the converters using the DirectFET devices whilst still not exceeding the specified 105°C maximum board temperature.

VII. RELIABILITY

New technologies that appear to be different to those that have preceded them sometimes cause concern over reliability. Consequently DirectFET technology has undergone extensive reliability testing to ensure that there will be no issues when it is working in applications in the field. The testing completed has included those tests that are commonly undertaken on power MOSFET components, as well as additional testing to show ruggedness and fitness for use.

In order to ensure that material sets used do not interact badly with the silicon die and that they also protect the die from the environment, bias testing is undertaken. High temperature reverse bias; temperature, humidity and bias; and high temperature gate bias have all been completed on large sample sizes (greater than 200) for 1000 hours with no failures. Additionally, thermal cycling tests including temperature cycling on board (-40 to +125°C) for 500 cycles and power cycling to 8000 cycles have been completed with zero failures. These tests are the standard tests that are completed by most vendors to qualify new power components. Further work has been undertaken to allay any mechanical strength concerns.

VIIa Bend strength measurements

An example of the additional testing that has been completed is bend strength measurement. Comparisons have been made with ceramic capacitors in order to determine how DirectFET technology compares to other components that it is likely to share a board with. There are standard tests to determine the strength of ceramic capacitors and these have been used on DirectFET devices. In all cases ceramic capacitors have also been tested as a control.

Bend strength measurements are simple in methodology - mount a device onto a board of pre-determined dimensions and then deflect and bend the

board about the point where the device is mounted. Continuous monitoring of gate leakage & gate threshold voltage allows the point of failure versus deflection to be determined. A photograph of the setup is shown in Figure 8.0.

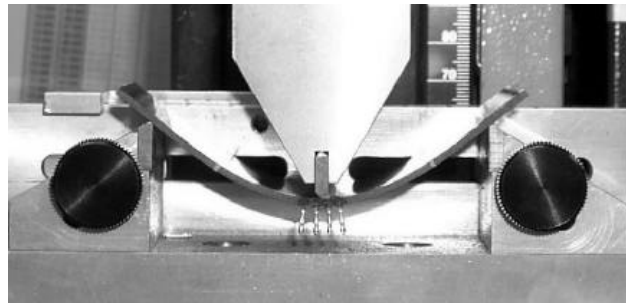


FIGURE 8.0. BEND STRENGTH MEASUREMENT SETUP (DIRECTFET DEVICE ON UNDERSIDE OF BOARD)

This testing was completed on DirectFET technology, investigating:

- orientation of device on board
- device on front and back of board
- thickness of board
- thickness of board attach solder
- composition of board attach solder

In all cases the ceramic capacitors failed (based on a 20% shift in capacitance) at a lower deflection than the DirectFET devices. This is shown in the set of mortality curves shown in Figure 9.0.

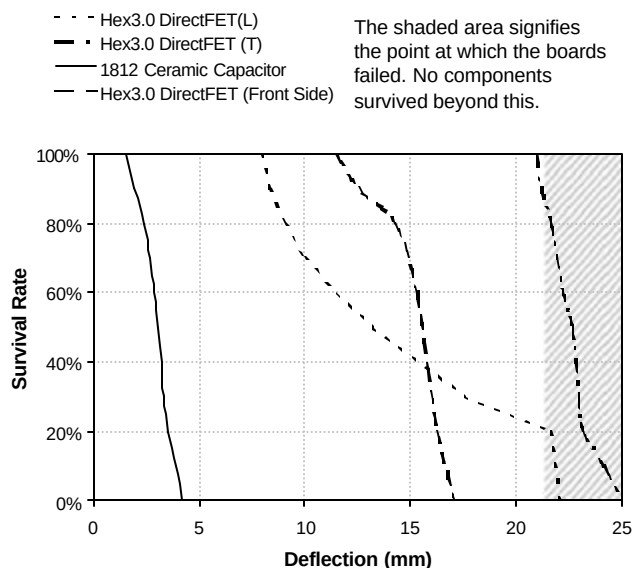


FIGURE 9.0 – MORTALITY CURVES COMPARING DIRECTFET TECHNOLOGY WITH CERAMIC CAPACITORS

In most of the tests the DirectFET devices did not fail catastrophically until the boards themselves snapped.

VIIb Compression resistance

In specifying that the device can be used in systems using dual sided cooling it is necessary to determine its fitness for this purpose. It was therefore necessary to investigate DirectFET technology's resistance to pressure. This was to ensure that heat sinking that applies a force to the top of the package would not result in damage. The testing again utilised continuous monitoring of gate leakage and gate threshold voltage whilst an increasing force was applied to the top of the package. No shifts in the monitored variables were observed below 500N. This figure is well above any force that would be used for mounting a heat sink. Typically these would not exceed 100N.

VIII. SUMMARY AND CONCLUSION

This paper has presented DirectFET technology, which is targeted at facilitating the current and power densities required by future power supplies for next generation microprocessors. Improvements in thermal and electrical conduction have been made through the rationalization of packaging design and tailoring it to the existing and future requirements of the synchronous buck converters used for processor power. These converters need to supply greater than 100A to the processors that they support. Multi-phase converters enable these high currents although each phase is still required to supply greater than 25A. Through in-circuit evaluations this paper has shown that the use of DirectFET technology facilitates greater than 30A per phase using a single device in each of the synchronous and control FET sockets in the converter. Alternate packaging platforms (e.g. SO-8) would require the paralleling of devices. Compared to existing best performing SO-8 devices DirectFET technology achieves double the current and power density whilst proving to be a reliable platform with fitness for purpose.