

# Application Note AN-1080

## DirectFET<sup>®</sup> Technology Inspection Application Note

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International Rectifier's DirectFET technology facilitates dual-sided cooling of surface mounted power MOSFET devices. This doubles power and current densities, which in turn reduces component count and system cost. These benefits result from the presence of solderable contacts on the surface of the silicon die for connecting the gate and source to the printed circuit board (PCB). A copper clip attached to the back of the die provides the drain connection. Devices in the DirectFET range vary but, typically, there are three electrical connections (gate, source and drain) but seven or more mechanical joints (one gate pad, one or more source pads, and four drain pads – each of the two drain rails is divided into two pads). This unique design means that inspection criteria for DirectFET devices may differ from more conventional surface mounted devices (SMDs). This application note explains the methods available for inspecting the quality of solder joints between device and PCB.

## Introduction

International Rectifier's DirectFET technology facilitates dual-sided cooling of surface mounted power MOSFET devices. This doubles power and current densities, which in turn reduces component count and system cost. These benefits result from the presence of solderable contacts on the surface of the silicon die for connecting the gate and source to the printed circuit board (PCB). A copper clip attached to the back of the die provides the drain connection. Devices in the DirectFET range vary but, typically, there are three electrical connections (gate, source and drain) but seven or more mechanical joints (one gate pad, one or more source pads, and four drain pads – each of the two drain rails is divided into two pads). Figures 1 and 2 show this construction.

This unique design means that inspection criteria for DirectFET devices may differ from more conventional surface mounted devices (SMDs). This application note explains the methods available for inspecting the quality of solder joints between device and PCB. Two other application notes, AN-1035 and AN-1050, describe the methods and practices required to board-mount DirectFET devices, and the interactions that may occur with commonly used materials. These documents are available at:

[www.irf.com/technical-info/appnotes/an-1035.pdf](http://www.irf.com/technical-info/appnotes/an-1035.pdf)

[www.irf.com/technical-info/appnotes/an-1050.pdf](http://www.irf.com/technical-info/appnotes/an-1050.pdf)

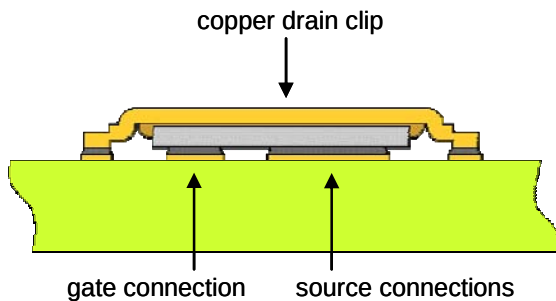


Figure 1 Side view of DirectFET device

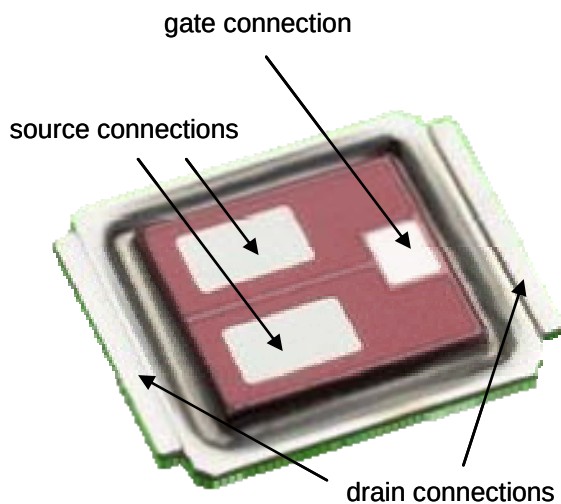


Figure 2 Bottom view of DirectFET device

## Inspection techniques

### Background

The drain connections on a DirectFET device are external, conventionally filleted solder joints (Figure 3). This means that they can be inspected visually, as with a conventional SMD, in accordance with industry standards (for example, IPC-A-610).

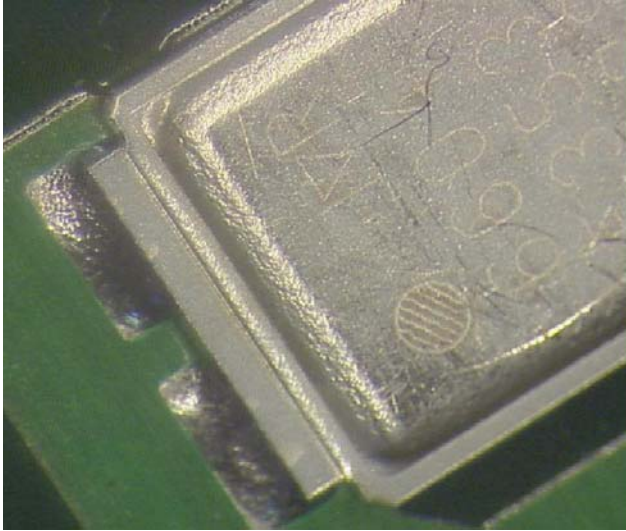


Figure 3 External solder fillets on the drain

However, as the direct gate and source contacts are within the outline of a DirectFET device, other inspection techniques are needed to inspect them with confidence. The most effective is X-ray microscopy.

### Optical inspection

Optical inspection can detect several possible assembly issues, including devices that are twisted, rotated, tilted, and both twisted and tilted at once.

Equipment is available that uses a camera to inspect Ball Grid Array (BGA) devices; it may be possible to use this to inspect the internal solder joints of a DirectFET device.

### X-ray inspection

Many manufacturers offer X-ray equipment, which may be batch or in-line, 2D or 3D.

It is unusual to inspect a whole production run using X-ray. It is more common to use this technique when setting up a process or product, and on samples taken from production runs.

## Examples of good assembly

Figures 4 to 6 show well-mounted DirectFET devices.

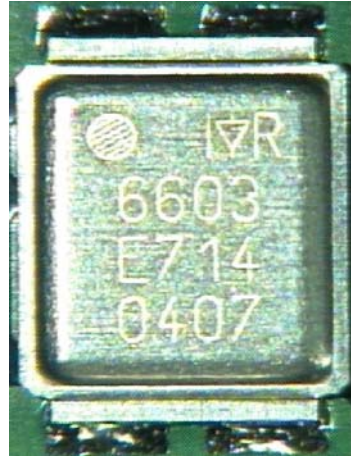


Figure 4 Self-centered with good solder fillets

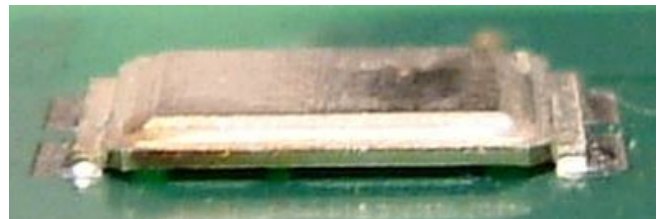


Figure 5 Device mounted parallel to PCB

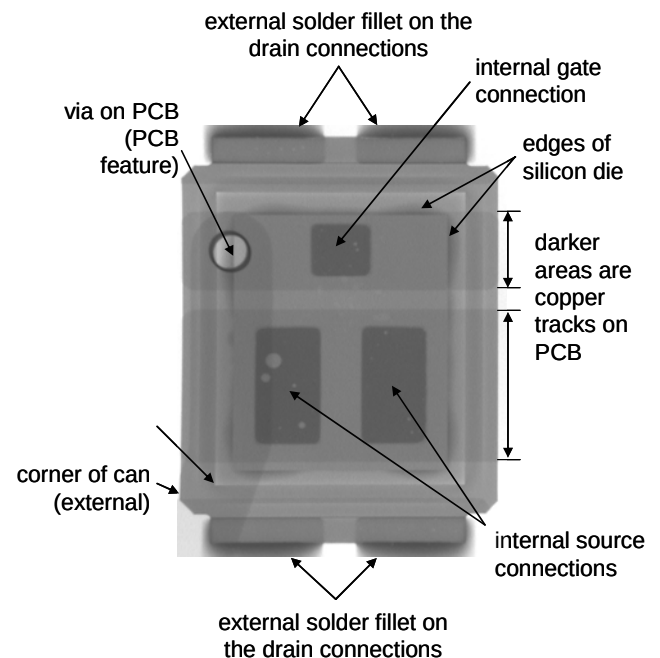


Figure 6 Features revealed by an X-ray

## Summary of rejection criteria

The remaining sections of this application note explain the types of problems that can arise when board-mounting DirectFET devices. In each case, criteria are given on which to base the decision whether to accept or reject a device. The table below summarizes these criteria and gives the number of the page on which you will find more information. As with all solder joints, a major factor in the success of joints on a DirectFET device is the applied solder volume. Too little solder may result in voided joints (or open circuits, in extreme cases) and too much solder may result in solder balling (or short circuits, in extreme cases).

| Observation               | Reject any device that has:                                                                                                                                                 | Page |
|---------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| Twisted device            | <p>A gate or source pad with less than 75% solder coverage</p> <p>A drain pad with less than 50% solder coverage</p>                                                        | 4    |
| Rotated device            | Been turned through 180°                                                                                                                                                    | 4    |
| Tilted device             | <p>A gate or source pad with less than 75% solder coverage</p> <p>A drain pad with less than 50% solder coverage</p> <p>Been tilted by more than 3° relative to the PCB</p> | 5    |
| Twisted and tilted device | <p>A gate or source pad with less than 75% solder coverage</p> <p>A drain pad with less than 50% solder coverage</p> <p>Been tilted by more than 3° relative to the PCB</p> | 5    |
| Solder voiding            | A solder joint with less than 75% coverage of the pad on the PCB                                                                                                            | 6    |
| Solder balling            | <p>A solder ball between the gate pad and the nearest drain pad</p> <p>A solder ball causing an electrical short</p>                                                        | 6    |
| Poorly formed joints      | A solder joint with less than 75% coverage of the pad on the PCB                                                                                                            | 7    |
| Open circuits             | A missing or open solder joint                                                                                                                                              | 8    |
| Short circuits            | A solder bridge linking electrically isolated points of the circuit (for example, between gate and drain pads not two drain pads)                                           | 8    |

Note: Some of the problems shown in this document were deliberately created for illustrative purposes. They do not commonly arise in practice.

## Types of faults

### Twisted device

This describes a device that is mounted crookedly on the pads, as shown in Figure 7. The device is clearly twisted but external solder fillets are still visible on all four drain contacts. The X-ray shows good solder joints on the gate and source contacts.

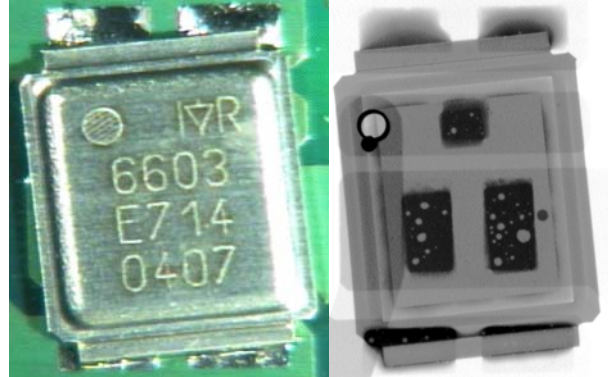


Figure 7 Twisted device

Reject twisted devices if one of the following is true:

- There is less than 75% coverage on gate or source contacts
- There is less than 50% coverage on drain contacts

### Rotated device

This describes a device that is mounted the wrong way around, as shown in Figure 8. Although the external solder fillets on the drain contacts are good, the X-ray reveals the problems with the gate and source contacts. You can see in the photograph that the device markings are upside down.

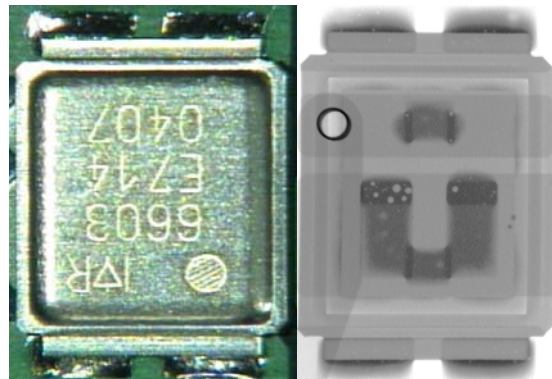


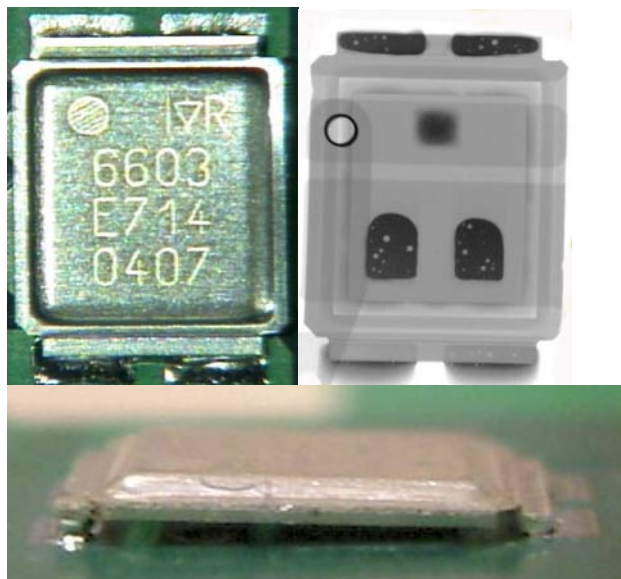
Figure 8 Rotated device

Reject all rotated devices.



### Tilted device

This describes a device that is not parallel to the PCB. Figure 9 shows an example. Although the device is self-centered, visual inspection from above reveals more solder on the bottom drain contacts in the photograph than on the top ones. This indicates a problem with the solder process: solder has been sucked underneath the device. Visual inspection from the side reveals that the device is tilted by more than  $3^\circ$  from the PCB. This again indicates a problem with solder under the device. The X-ray confirms the problem; it also reveals that the gate contact is not made and the tops of the source contacts are indistinct, indicating that the joints are tapered.



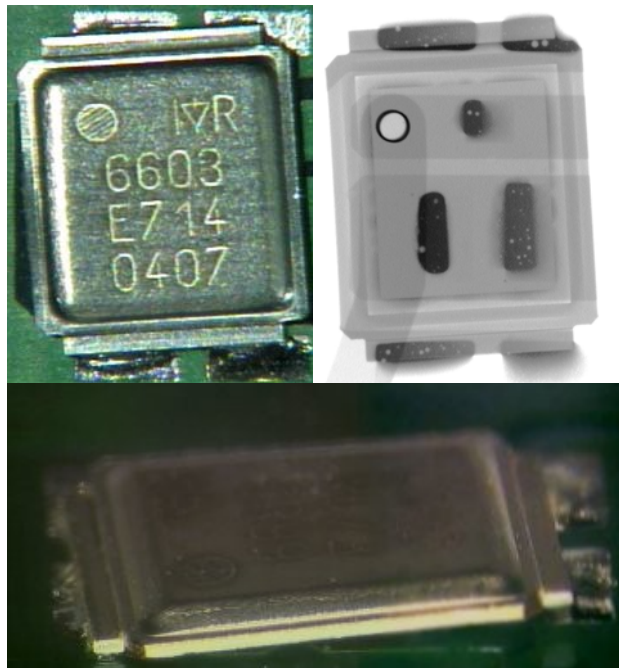
*Figure 9 Tilted device*

Reject tilted devices if one of the following is true:

- There is less than 75% coverage on gate or source contacts
- There is less than 50% coverage on drain contacts
- The angle of tilt exceeds  $3^\circ$

### Twisted and tilted device

This describes a device that is both crooked on the pads and not parallel to the PCB (Figure 10). Visual inspection from above reveals the twist and from the side reveals the tilt. The X-ray shows the combined effects, with the contact area reduced by the twist and the pad definition impaired by the tilt. The contacts on the right side of the device are poorly made.



*Figure 10 Twisted and tilted device*

Reject twisted and tilted devices if:

- There is less than 75% coverage on gate or source contacts
- There is less than 50% coverage on drain contacts
- The angle of tilt exceeds  $3^\circ$

## Solder voiding

This describes joints in which some areas have no solder, as shown in Figure 11. Voids are less common with lead-free devices (PbF suffix on part number) because pre-soldering makes joints more consistent.

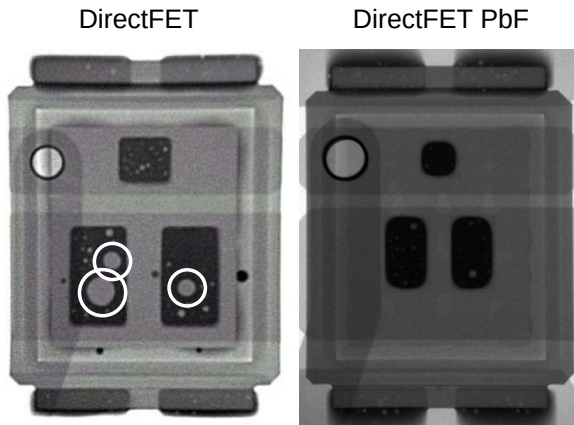


Figure 11 Examples of solder voids

Many industry standards (for example, IPC-A-610) accept voiding levels of up to 25% of the joint area. International Rectifier has carried out reliability tests on devices with 30% solder voiding that showed no deterioration in parametric or long-term reliability testing results.

To evaluate accurately the degree of solder voiding, it is important to use imaging and/or pixel-counting software. Estimating a percentage intuitively from an image invariably leads to inaccurate, usually exaggerated, results. Typically, people tend to judge the level of voiding to be about double the true amount. Figures 12 and 13 show two examples where viewers estimated about 20% of the contact area to be affected but imaging software revealed the true value to be only 12-13%. This demonstrates the importance of good image analysis software.



Figure 12 Voids on the gate contact



Figure 13 Voids on the left source contact

## Solder balling

This describes spheres of excess solder left after reflowing (Figure 14). In its most extreme form, it may result in short circuits.

As with any SMD, the aim in assembling DirectFET devices is to achieve good solder coverage of the joint area without solder balling. However, it is not always possible to achieve the ideal amount of solder, and solder balls sometimes form. In addition to solder quantity, an incorrect reflow profile (ramp rate too high) can cause solder balling; this happens because the solvent and/or flux boils, ejecting solder particles from the body of solder.

Although solder balling is not desirable, a few solder balls need not necessarily be an issue. There is no evidence to suggest that solder balling impairs the function, performance or reliability of DirectFET devices. This is because, once the device has been mounted, any solder balls cannot move to an area where they will cause an electrical short. In addition, the die surface is covered with a passivation material that protects it.

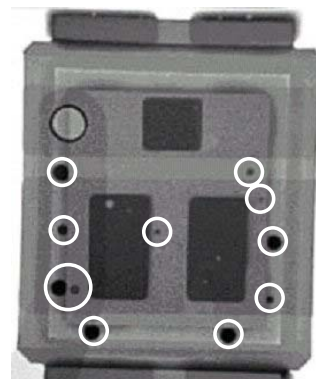


Figure 14 Examples of solder balls

Only a solder ball next to the gate pad, as shown in Figure 15, is likely to present problems. Although the ball will not itself cause an electrical short, a smear of flux, solder particles or contaminant could lead to an electrical short or leakage in certain circumstances. This is very rare but can be exacerbated if the device shifts during reflow.

Solder balling is less common with lead-free devices (PbF suffix on part number) because pre-soldering makes joints more consistent.

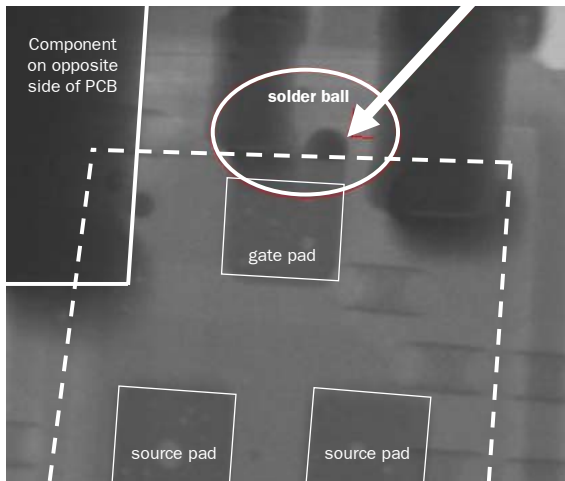


Figure 15 Example of a problematic solder ball

When inspecting solder balls, consider:

1. **Position** Solder balls are a concern only when they occur next to the gate pad, between it and the closest drain pad.
2. **Shorting** Use electrical tests to check for shorts. If there are no shorts when the device is mounted, there is no evidence to suggest that solder balls can cause shorting later.

The number and size of solder balls is not important. However, if solder balls occur often, use SPC (Statistical Process Control) techniques to identify and address the cause.

### Poorly formed joints

This describes joints in which the full area of the pad is not in contact. In its most extreme form, it may result in open circuits. Poorly formed solder joints appear on X-ray images as irregular patterns and shapes, as shown in Figure 16.

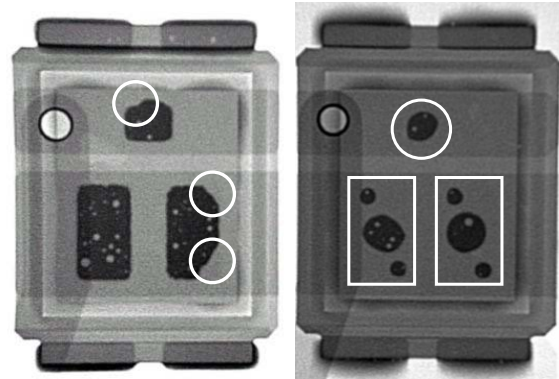
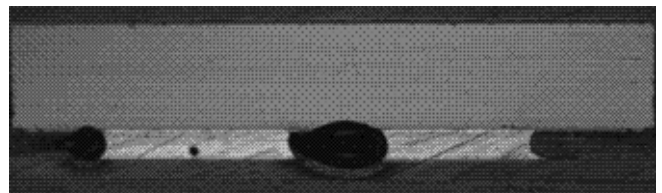


Figure 16 Examples of poorly formed joints

However, joints on lead-free devices (PbF suffix on part number) are less clearly defined than on standard devices (Figure 11). The solder thickness is typically 145µm instead of 75µm and the solder flows freely over the pre-soldered pads. This results in the joint tapering from its widest points on the device and substrate to its narrowest point halfway between them (Figure 17). As X-rays show the solder quantity, the edges of joints appear less dark than their centers.

DirectFET



DirectFET PbF

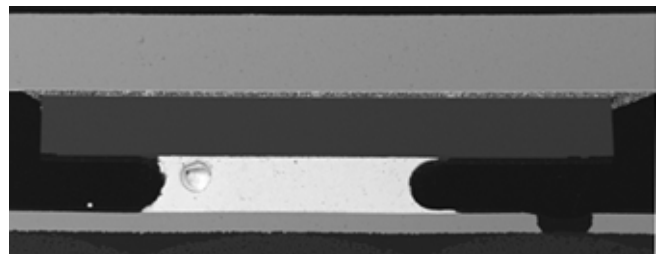


Figure 17 Cross-sectional views of solder joints



Poorly formed joints are acceptable unless the area affected exceeds 25% of the joint. There is no need to rework or reject devices until this level is exceeded. However, if poor joints often occur, use process engineering or optimization and yield improvement exercises to rectify the situation.

As with voiding, use imaging or pixel-counting software to evaluate the extent of the affected area. Figures 18 and 19 show examples.



Figure 18 Poorly formed source joint – 11% missing

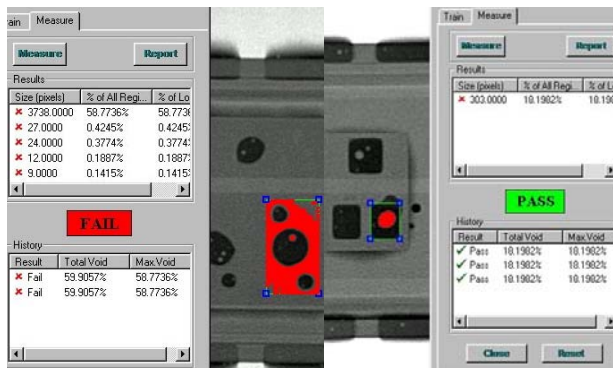


Figure 19 Fail (60% missing) and pass (18%) results

### Open circuits

This describes failed joints where there is no electrical connection. Open circuits appear on X-ray images as pads that are faint and/or poorly defined. Figure 20 shows two examples of open circuits:

1. The image on the left shows an open connection on a source pad. There is no electrical connection so this device would have to be rejected or reworked.
2. The image on the left shows a drain rail where one of the two pads is open. This should be rejected because it has a maximum of 50% coverage, even if the other joint is perfect.

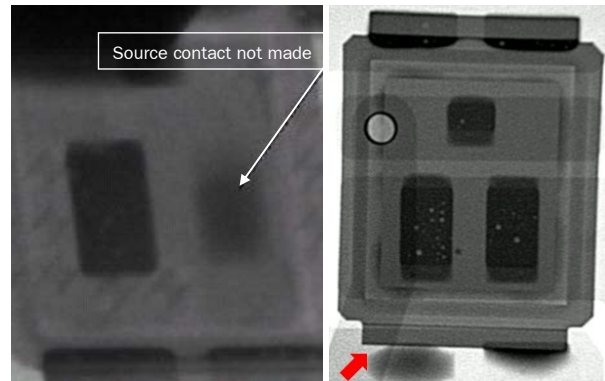


Figure 20 Examples of open circuits

### Short circuits

This describes accidental electrical connections between contacts that should be isolated. Like solderballing, it results from excess solder. Figure 21 shows two examples of short circuits:

1. The image on the left shows a solder bridge between the source pads. Although this is undesirable, it is acceptable because the pads are electrically common.
2. The image on the right shows a solder bridge between the gate pad and a track on the PCB. This must be rejected or reworked. It might be detected in electrical testing if not by X-ray.

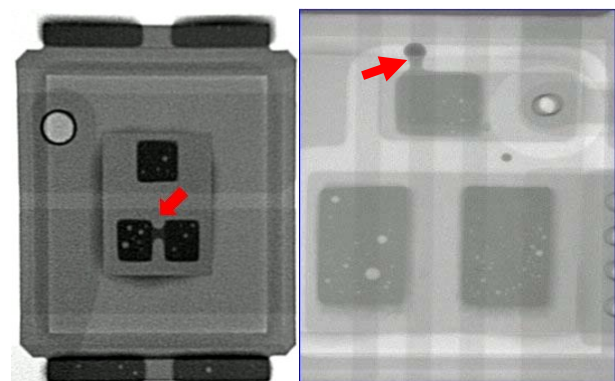


Figure 21 Examples of short circuits



## Design issues

In addition to their role in inspecting for processing faults, X-rays can reveal board design issues.

Figure 22 shows the gate pad on the PCB extending beyond the edge of the die. Although the border of passivated silicon between the edge of the gate contact and the edge of the die on the device should prevent problems from arising, PCB pads should be defined accurately.

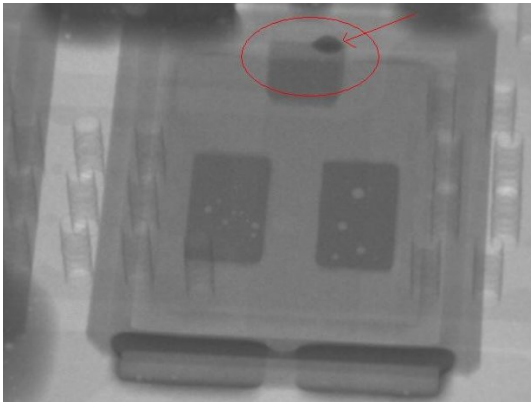


Figure 22 Over-sized gate pad on PCB

Figure 23 shows poor edge definition on solder joints. The cause is the lack of a solder mask to define the gate and source pads; they are defined only by the edge of the copper track.

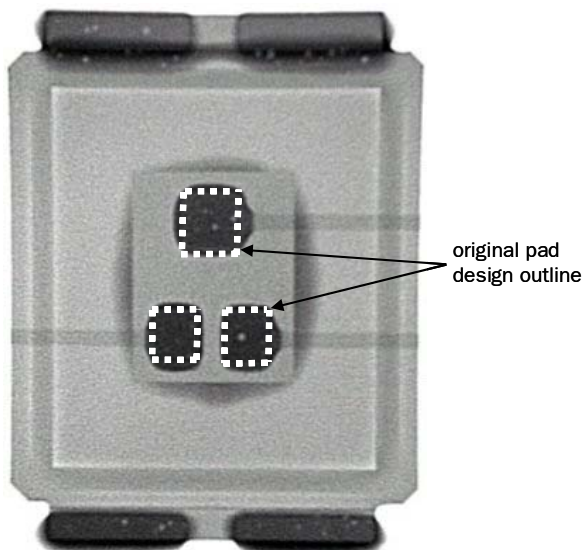


Figure 23 Absence of a solder mask to define pads