Designing the NEWCARD Connector Interface to Extend PCI Express Serial Architecture to the PC Card Modular Form Factor

Abstract

This paper provides information about the NEWCARD connector and board design considerations that need to be addressed to implement PCI Express architecture in add-in module applications similar to those supported by PC Card today. The high-speed electrical performance requirements for the connectors to support NEWCARD Generation 1 and Generation 2 data rates will be described. These requirements include insertion loss, return loss and near-end crosstalk. Generation 1 requirements define performance up to 2.5Gb/s. Generation 2 scales performance to 6.25 Gb/s. The presentation will also address how these demands can be met. Simulation of the connector crosstalk will be shown and compared to actual measured data. Implications of the high-speed signaling requirements on connector mechanical design will be explained. Board design guidelines to optimize electrical performance will be provided to assist designers with implementation in add-in modules and client systems. This paper provides guidelines for System Designer, System Manufacturer, Standards and SIG Representatives to implement the NEWCARD connector into their current and future designs.

Contents

Introduction

The evolving demands of client platforms will exceed the capabilities of the traditional PCI parallel bus. The NEWCARD interface will enable the implementation of the high-speed serial PCI Express architecture for add-in modules used with mobile and desktop platforms. The NEWCARD host interface will initially support a single PCI Express lane at 2.5Gb/s and must be capable of extension to second-generation speeds of 6.25 Gb/s. The interface must also support USB 2.0 for ease of integrating popular peripheral functions. The transition to PCI Express architecture is creating new product opportunities for computer OEMs, add-in card manufacturers and connector suppliers. Client OEMs and card manufacturers are challenging connector manufacturers to develop compact, cost-effective, and reliable NEWCARD solutions to enable high-performance, add-in modules for thin-and-light notebooks and small-form-factor desktops.

In order to attain these high data rates care must be taken in the design and implementation of the connector, as well as the Printed Circuit Board (PCB).

Electrical Requirements

There are three important electrical parameters that will be affected by the increase in signal speeds as we migrate to the next generation client platforms; Insertion Loss, Return Loss and Near End Crosstalk (NEXT). These three parameters will not only be determined by the connector, but can also be influenced by the PCB as well if signal integrity rules are not observed in the early stages of the board design. In order to understand how the increase in speed affects the above parameters a brief definition will be presented for each of them below.

Insertion Loss

Insertion loss is a measure of how much of the input energy is transmitted through the system to the output. When a reflection occurs on the line not all of the energy is reflected back to the input; some of it is transmitted with a voltage amplitude given by a transmission coefficient T. The insertion loss is usually defined in dB with the following equation:

$$IL = -20 \log |T| \text{ dB} \qquad (1)$$

Where: $T = 1 + \Gamma$

The total Insertion Loss is affected by reflections, as well as dielectric losses of the PCB material, the plastic that is used in the connector, and conductor losses. All of these contributors will decrease the amount of signal measured at the output. Figure 2 shows a typical plot of what Insertion Loss would look like. Less Insertion Loss is “good” and shows up as less negative on an Insertion Loss plot.

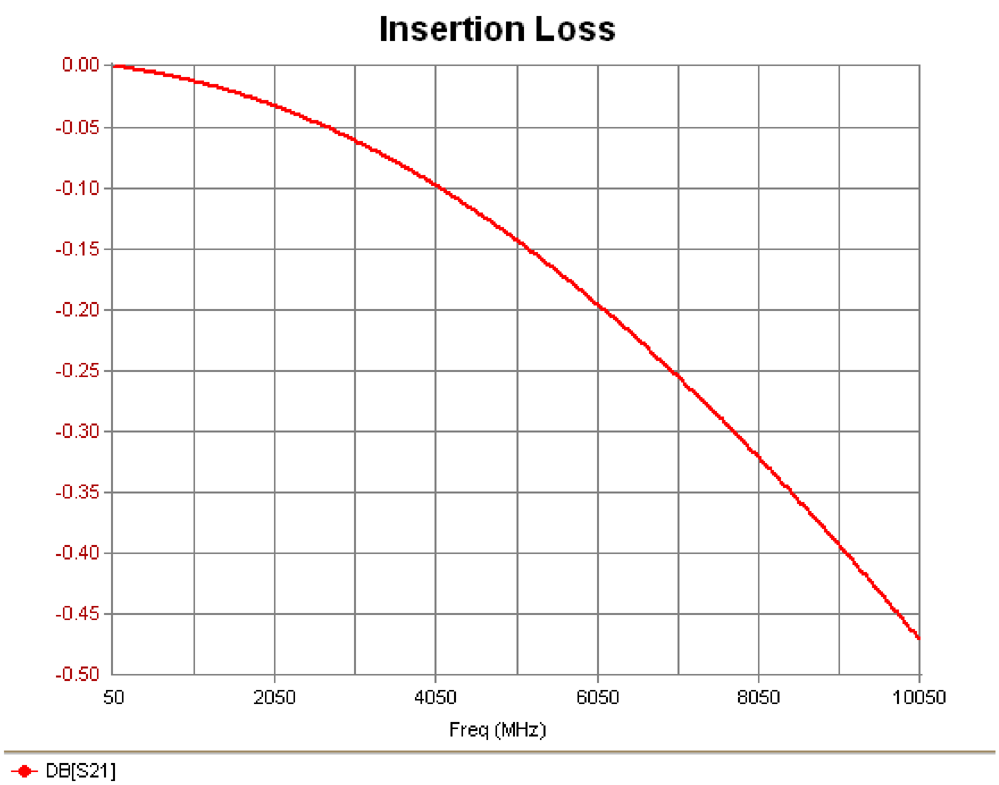

Figure 2 Typical Insertion Loss Plot

Return Loss

When there is a mismatch between the load at the far end of the line and the source at the near end of the line some energy is reflected, and not all of the available power from the source is delivered to the load. This "loss" is defined as the return loss. In other words, return loss is a measure of how much energy is reflected back to the input. The return loss is usually defined in dB with the following equation:

$$\text{Return Loss} = -20 \log |\Gamma| \text{ dB} \qquad (2)$$

Where: $\Gamma = (Z_L - Z_O) / (Z_L + Z_O)$

Z_o = Characteristic Impedance

Z_L = Load Impedance

Γ = Reflection Coefficient

From the above definition it is easily shown that changes in the characteristic impedance within the connector, and the PCB by themselves, or the change in impedance at the connector to PCB interface will have a direct effect on the return loss.   Figure 1 shows an example of a typical Return Loss plot. Greater Return Loss, which corresponds to a smaller reflected signal, is "good", and shows up as a more negative result in a Return Loss plot.

Figure 1 Typical Return Loss Plot

Near End Crosstalk (NEXT)

Crosstalk is caused by coupling of energy from one part of the circuit to another. There are two mechanisms that cause crosstalk; mutual inductance and mutual capacitance.

Mutual inductance generated from a driven line will induce a noise voltage onto a victim line proportional to the rate of change in current in the driven line. Since the noise is proportional to the rate of change, mutual inductance becomes very significant in high-speed applications that change states from a high to a low at picosecond speeds.

Mutual capacitance generated from a driven line will inject a noise current onto a victim line proportional to the rate of change in voltage in the driven line. Again, since the noise is proportional to the rate of change, mutual capacitance is very important in high-speed applications as well. A typical plot of the NEXT would look somewhat like that of the return loss plot and has been omitted here.

NEWCARD Generation 1 and Generation 2 Signaling Requirements

The following are the current high-speed requirements set forth by the NEWCARD committee:

- **Insertion Loss:** **Gen.1** ~ < -0.75dB up to 1.25GHz
  Gen.2 ~ < -0.75dB up to 3.125GHz
  and < -4dB up to 6 GHz
- **Return Loss:** **Gen.1** ~ < -12dB up to 1.25GHz
  Gen.2 ~ < -12dB up to 3.125GHz
  and < -5dB up to 6 GHz
- **NEXT:** **Gen.1** ~ < -32.0dB up to 1.25GHz
  Gen.2 ~ < -32dB up to 3.125GHz
  and -26dB up to 6GHz

Connector Considerations

The impedance of the connector could be considered as one of the most important parameters to meet. If you are working in a 100 ohm differential system the closer the connector is to this value the less loss you will have, the less reflection you will have, and this in turn will reduce the amount of crosstalk that is generated. It is difficult if not impossible to design a connector that is exactly 100 ohms throughout its entire signal path (tail to tail). This is due in part to the other mechanical features that need to be designed into the connector, as well as the plastic housing that is needed to hold the contacts in place. However, there are some techniques that can be utilized in order to “tune” the impedance of the connector closer to the desired value.

To obtain a constant impedance through the connector tradeoffs, can be made on design features, such as the normal force, geometry of the contact, placement of plastic to hold the contact. Since most of the loss associated with the connector is due to reflections it is important that the connector have an impedance profile that is as flat as possible. Breaking the connector geometry down into small sections will allow the designer the ability to inspect the impedance at every point along the signal path. This will insure that the best possible impedance profile is obtained throughout the entire connector. The signaling speeds required for the NEWCARD connector are fast enough that pieces of geometry down to approximately 1.12mm in length can have an effect on the performance. There is an interface between the connector and the PCB which also needs to be tuned as close to the system impedance as well. Having a perfectly tuned connector that enters a PCB with a large difference in impedance will cause a large discontinuity resulting in poor system performance.

PCB Considerations

The choice of dielectric material is an important factor when designing a PCB to operate at the NEWCARD speeds. Materials with a lower loss tangent and lower dielectric constant will reduce the amount of loss of usable signal. However, this will come at an increased cost. There is a difference of 2:1 in cost when migrating from the traditional FR4 material to Roger4350 – Rogers material has been chosen for high-speed qualification testing by the NEWCARD Test Working group. Length of trace will also be a factor in deciding what material is best suited for your application. The average loss in standard FR4 material is about -0.3dB/in @ 1000Hz. Therefore, for traces that need to be routed over a long distance, dielectric materials with a low loss tangent and dielectric constant should be considered. The insertion loss specification for the Generation 2 connector is -0.75dB, which means most of the loss associated with your NEWCARD design will likely be attributed to the printed circuit board rather than the connector if you are going to use FR4. Your system specification will determine which board material is right for you.

The NEWCARD specification states that the electrical parameters described above include the effects of the connector as well as the pads on the PCB where the connector attaches. With this in mind, there are some practical considerations that need to be addressed. One of the first things that should be thought about is how the testing will be performed. The electrical characteristics can all be measured using a Vector Network Analyzer (VNA). However, there are several different ways of attaching the test equipment to the device under test (DUT). Currently, the NEWCARD committee is working on two different methods; SMA attach and probing.

If SMA attach (Figure 3) is used, then care must be taken when laying out the test traces so that the least amount of discontinuities are encountered. It is also good practice to locate calibration traces as close to the test traces as possible to avoid any variation in the PCB dielectric that would change the response of the test traces vs. the calibration traces. The calibration traces can be used to de-embed the connector/pads from the measurement. This can be done by subtracting out the effect of the calibration traces from the full system measurement.

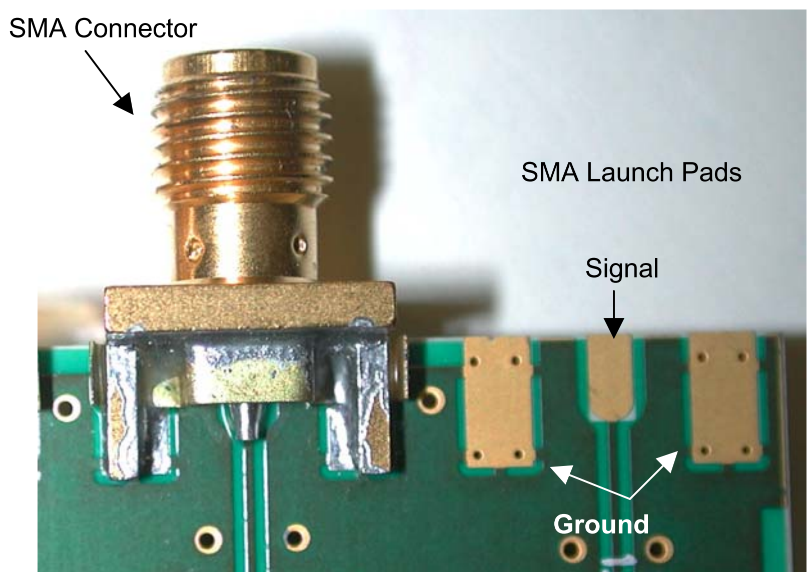

Figure 3 Example SMA Launch

Probing is an alternative method of measuring the NEWCARD connector response. This method can be used to reduce the discontinuity associated with the SMA. Using this approach, you are able to use smaller lengths for the test traces, which will reduce the amount of loss associated with the test board. In this technique you will also need calibration traces so that the lengths of trace used can be removed from the measurement. Figure 4 shows an example of a probe pad launch.

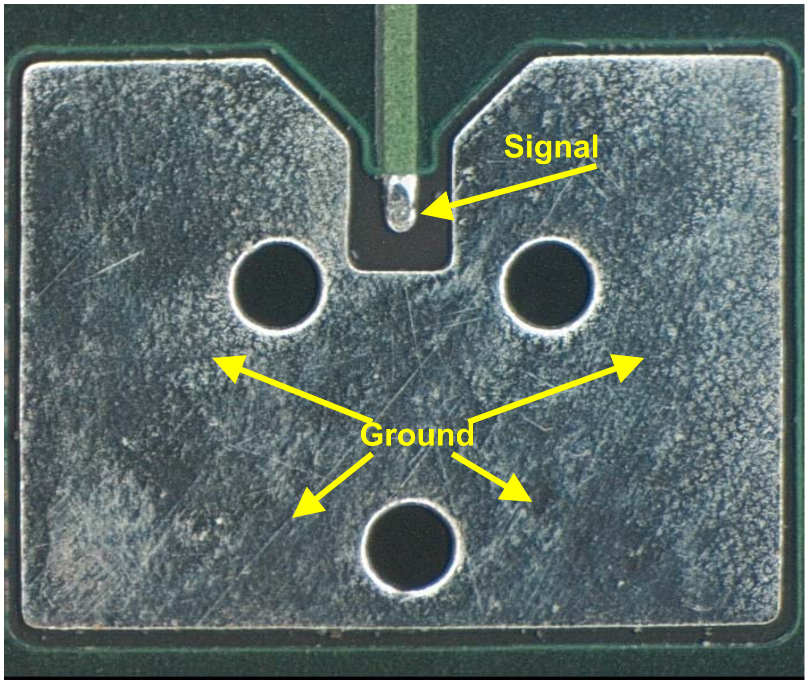

Figure 4 Probe Pad Launch

Care should be taken in both techniques to avoid large discontinuities at the SMA launch pads, or the probe launch pads.

Testing and Validation

Both SMA and probe launches were fabricated onto the test board so that either method could be used for the NEWCARD validation. Unfortunately, testing was only performed on the NEWCARD connector using the SMA method discussed above due to manufacturing problems that were encountered with the probe launch. Figure 5 shows a representation of the problem that arose. The solder mask applied to the PCB's improperly covered too much of the signal trace, which in turn did not allow enough skate for the probe. In other words, the probe could not properly seat itself on the signal pad. This problem will be eradicated on the final version of the test boards that will be used for the qualification testing.

All of the data that is presented was taken via a four-port measurement on the test sample utilizing a VNA. The time domain data was generated by transforming the frequency domain data using a proprietary MatLab script.

Figure 6 shows the resulting Insertion Loss that was measured. The graph includes the current specification in RED so that the level of performance obtained can be compared to the requirement. The traces on the test board were designed to be 50 ohm single ended uncoupled microstrip, rather than 100 ohm coupled differential traces. Figure 7 illustrates the complete test sample, including the trace layout, as well as the connector with the module test card inserted.

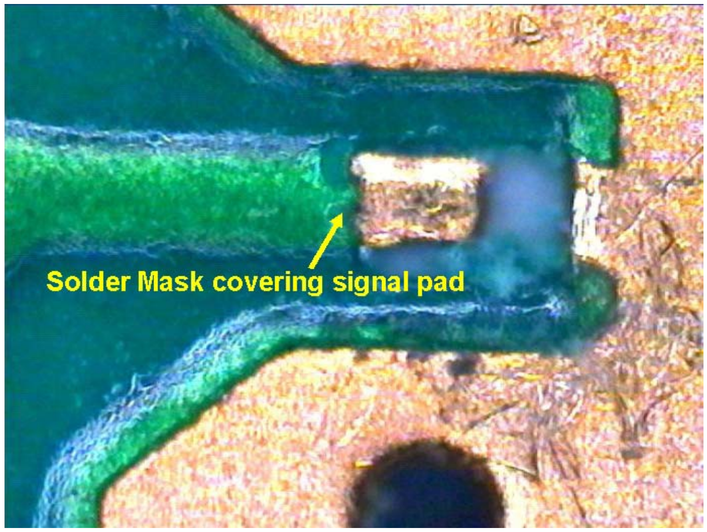

Figure 5 Magnified Probe Launch Showing Lack of Skate on Signal Trace

A calibration trace was included on the test board for both the probe launch and the SMA launch. The NEWCARD connector is being proposed as a differential solution. However, the calibration structure consisted of a single trace with the combined length of the signal traces from both the host board and module card. Since the signal test traces were designed as 50 ohm uncoupled microstrips it was not necessary to layout a set of differential calibration traces. The data shown in Figure 6 is that with the loss of the test traces removed. The dip in the plot at about 2.7GHz is very close to the requirement, but is still within the specification.

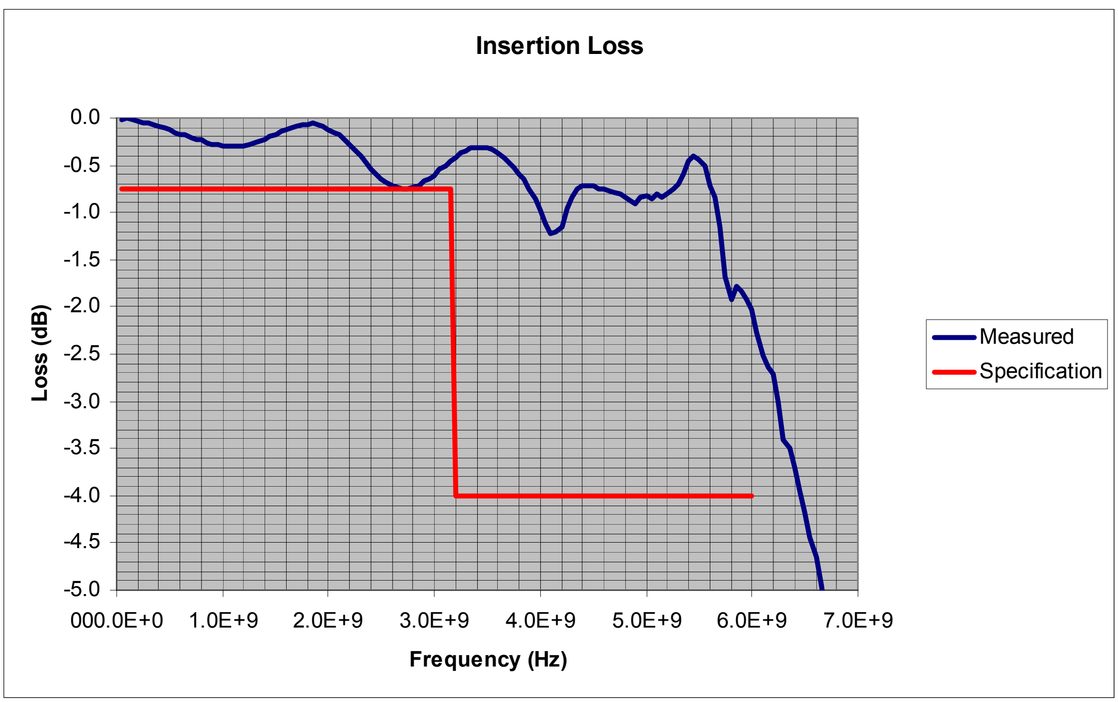

Figure 6 Insertion Loss Results

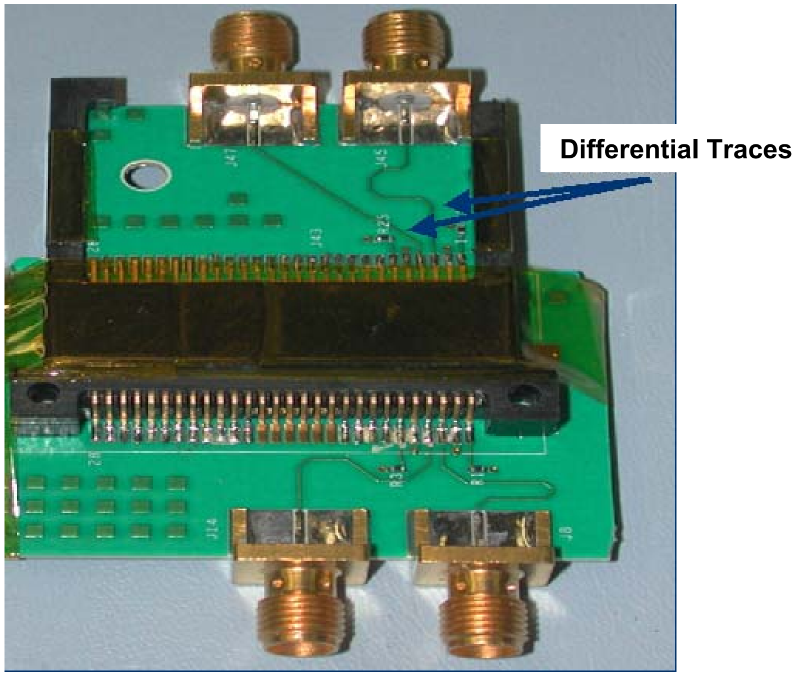

Figure 7 Complete NEWCARD Test Sample

The results of the return loss testing are shown in Figure 8. Again, the RED line indicates the requirement set forth by the NEWCARD committee. The yellow circle in the figure points out that the results are higher than the specified value at about 2.7GHz. The null in insertion loss at this same frequency would seem to indicate that there is an impedance reflection problem in the test sample.

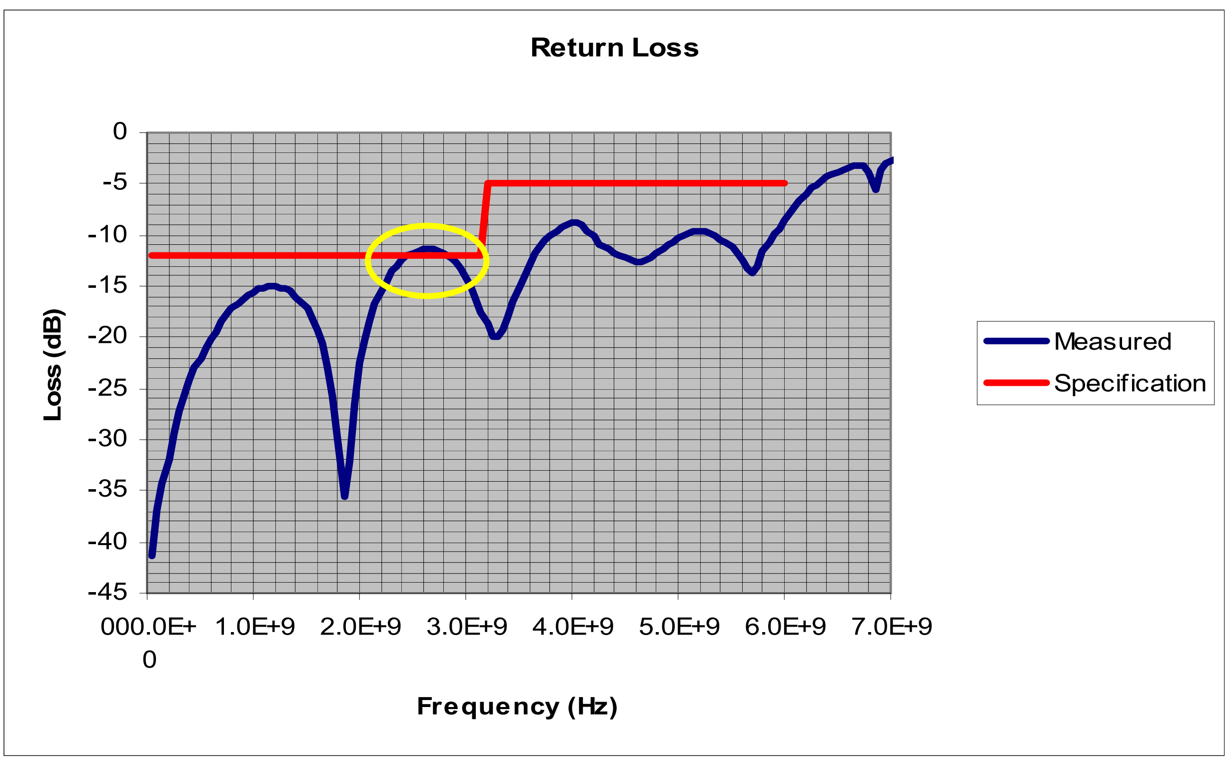

Figure 8 Return Loss Results

Transforming the return loss result into the time domain will show what the impedance profile looks like so that the reflections can be examined more closely. Figure 9 is a time domain representation of the reflections. The rise time used to generate this plot was 40ps.

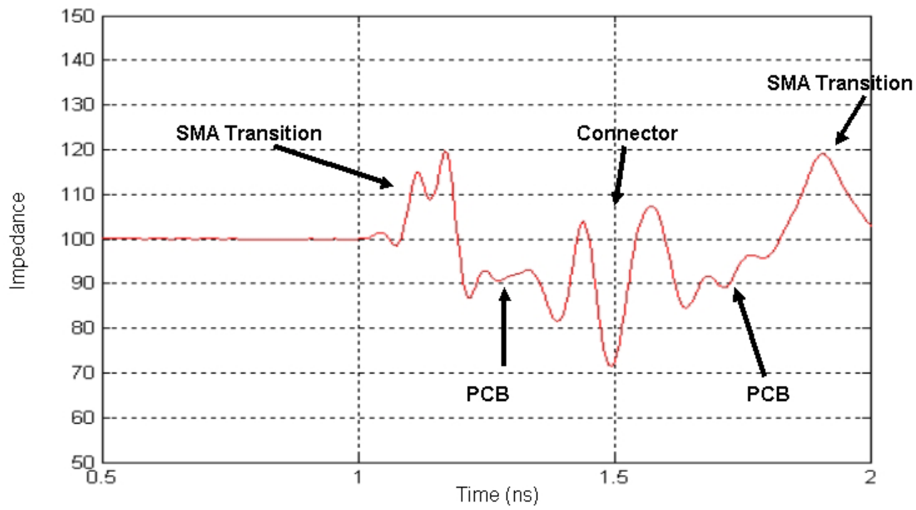

Figure 9 Time Domain Plot of Impedance

It is clear from this plot that the SMA transition induces quite a large discontinuity (reflection) in the system. It is possible that this launch point could be the cause of the large return loss maximum pushing the measurement out of spec. Due to time constraints at the time of this writing, and the availability of tests samples no further investigation was performed. However, the NEWCARD test working group is currently working on this problem and is sure to alleviate it by one of 2 methods:

1. There is a possibility that that the proposed specification was set more stringent that it needs to be based on the end use of the NEWCARD technology. This will translate into the return loss specification being relaxed a bit from its current value.

2. The reflections caused by the launches on the test board will be re-designed and a new set of boards will be fabricated so that further testing can be performed.

The near end crosstalk (NEXT) test result along with the simulated crosstalk is shown in Figure 10. The testing revealed that there is no problem meeting the specification set by the NEWCARD committee for the NEXT. The model used for the simulation did not include the test board that was used in the testing. Modeling was performed on the connector only. This helps to explain the lack of correlation between the simulated and measured results. Examining the low value of crosstalk obtained in the measurement hints to the validity of the assumption that the traces are truly uncoupled.

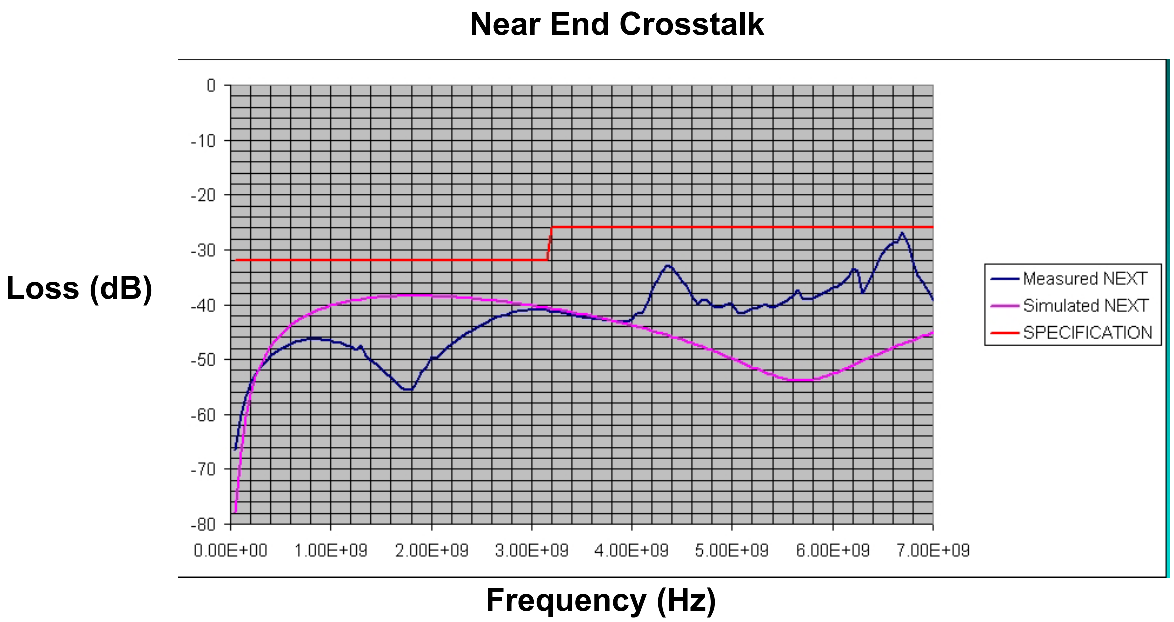

Figure 10 Near End Crosstalk Results

Conclusions

The proposed design should be able to meet the 0.7 draft requirements for Insertion Loss, Return Loss and NEXT, as long as the Return Loss problem can be eradicated.

Based on the Return Loss results it is obvious that careful attention to signal integrity should be given to the PCB in all NEWCARD applications to avoid loss of signal quality.

Feedback

- To provide feedback about adapting a NEWCARD solution for your system, please send an e-mail to dsideck@fciconnect.com or, cclewell@fciconnect.com
- For more information specific to NEWCARD technology refer to the PCMCIA website located at: http://www.pcmcia.org